

Optimization of an On-chip Active Cooling System Based on Thin-film Thermoelectric Coolers: Extended Discussion

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Abstract— In this paper, we explore the design and optimization of an on-chip active cooling system based on thin-film thermoelectric coolers (TEC). We start our investigation by establishing the compact thermal model for the chip package with integrated thin-film TEC devices. We observe that deploying an excessive number of TEC devices and/or providing the TEC devices with an improper supply current might adversely result in the overheating of the chip, rendering the cooling system ineffective. A large amount of supply current could even cause the thermal runaway of the system. Motivated by this observation, we formulate the deployment of the integrated TEC devices and their supply current setting as a system-level design problem. We propose a greedy algorithm to determine the deployment of TEC devices and a convex programming based scheme for setting the supply current levels. Leveraging the theory of inverse-positive matrix, we provide an optimality condition for the current setting algorithm. We have tested our algorithms on various benchmarks. We observe that our algorithms are able to determine the proper deployment and supply current level of the TEC devices which reduces the temperatures of the hot spots by as much as 7.5 °C compared to the cases without integrated TEC devices.

I. INTRODUCTION

AS THE manufacturing technology steps into the nanometer regime, power density has become a limiting factor for integrated circuit design. Heat dissipated highly unevenly in the active silicon layer, with the peak localized heat fluxes ($> 300 \text{ W}\cdot\text{cm}^{-2}$) being an order of magnitude larger than the average value across the entire chip [1]. This creates high temperature spots, posing threats on the reliability and performance of the entire chip. Thus, removal of the high-density heat fluxes becomes a crucial task of the chip cooling systems.

Most of the current cooling technologies fall into the category of *passive cooling*, where heat produced by the chip is removed via conduction and convection. In order to improve the efficiency of the heat exchange system, remarkable progress has been made in recent years in the development of heat transport materials and advanced heat exchanger structures such as nanotubes and microchannels [2, 3]. These passive cooling technologies are most effective in removing heat from bulks where heat is distributed evenly. However, they are not as efficient when the chip presents high

degrees of spatial power density variation. The inability to provide localized cooling at the hot spots might result in over-design of the heat exchange system, leading to excessive cooling cost. Cooling cost is already a major item in overall system cost. In data centers, the cooling energy cost has surpassed the energy consumption of the computation equipment [1].

On the other hand, by making use of specially designed miniature heat pumps, *active cooling* technologies can provide site-specific and on-demand cooling, promising new opportunities in cost effective cooling [1, 4-6]. More profoundly, the capability of providing tunable cooling at a fine granularity has significant implications on the thermal aware design of the entire chip. Potentially, the active cooling system, the thermal monitoring system, and the architecture-level thermal management mechanisms [7] can operate synergistically to achieve enhanced performance under a safe operating temperature.

In order to bring this vision into reality, two major hurdles need to be overcome, namely the technology for manufacturing on-chip active coolers and design automation of the cooling system. Recently, intensive research effort has been devoted to multiple candidate active cooling schemes, including integrated thermoelectric cooler (TEC) [1, 6], mini-scale vapor compression [8], and miniature capillary pump loop [9]. Among these techniques, integrated TEC is the most accessible one. Off-the-shelf macroscopic TEC devices have long been available [10]. Very recently, Intel researchers have demonstrated the first viable on-chip thin-film TEC manufacturing technology, which has the potential to enable a wide range of currently thermally limited applications [1].

In spite of these promising results in the manufacturing technology, system-level design automation of active cooling system remains largely unexplored. In this paper, we investigate the design and optimization of an on-chip active cooling system based on the recently developed super-lattice thin-film thermoelectric coolers [1]. More specifically, we focus on the following active cooling system configuration problem: Identifying (1) the deployment of TEC devices, i.e. the regions of the silicon layer that need to be covered by TEC devices; (2) the supply current setting of the on-chip TEC devices. The resulting cooling system should guarantee the operating temperature to remain within the allowable range under the worst-case power profile. We propose an optimization framework for this problem and have tested it

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using various benchmarks. We observe that our algorithm was able to bring down the temperatures of the hot spots by as much as 7.5 °C (compared to the cases without integrated TEC devices). The total power consumption of the resulting cooling system is reasonably small (around 2 W). Moreover, for all benchmarks, the execution time of our algorithm is less than 3 minutes.

In summary, our contribution lies in the following aspects:

- We conduct the first architectural level study of the active cooling system based on integrated TEC devices;
- We reveal the cooling system thermal runaway phenomenon;
- We propose a greedy deployment algorithm and a convex programming based supply current setting algorithm;
- We lay out the theoretical foundation for the analysis of the thermoelectric cooling system by extending the theory of inverse-positive matrix [11].
- We analyze the optimality of the current level configuration algorithm using our proposed thermoelectric cooling system analysis framework.

The remainder of the paper is organized as follows. Section II gives an overview of the related works. In Section III, the design of an on-chip active cooling system based on thin-film thermoelectric coolers is presented, followed by the in-depth discussion of our proposed compact thermal model of the entire chip package in Section IV. We introduce the optimization framework for the cooling system in Section V. Experimental results are presented in Section VI. Finally, we conclude our work with a summary in Section VII.

II. RELATED WORKS

There has been a few early-stage works concerning the optimization of TEC devices. Abramzon examines the optimal parameters (such as the height/area ratio) for a single TEC device using a numerical optimization approach [12]. Hou *et al.* propose an analytical framework to determine the optimal height of the TEC devices [13]. These works concentrate on the optimization of the physical parameters of the TEC devices. To the best of our knowledge, our work is the first attempt to systematically study the system level optimization problem of the integrated TEC-based active cooling system and evaluate the impact of the active cooling system on the overall thermal behavior of the entire chip package.

III. ACTIVE COOLING SYSTEMS LEVERAGING THIN-FILM THERMOELECTRIC COOLERS

A. Basics of Thin-Film Thermoelectric Cooler

A TEC device is typically composed of a couple of dissimilar semiconductor strips connected electrically in series and thermally in parallel (Figure 1(a)). The principle behind the thermoelectric cooler is the Peltier effect: when an electrical current is sent through the strips, heat is absorbed on one side and released at the other side. Denoting the heat flux absorbed from the cold side as q_c and dissipated from the hot side as q_h at temperatures θ_c and θ_h , respectively, the following equations describe the principle of thermoelectric cooling

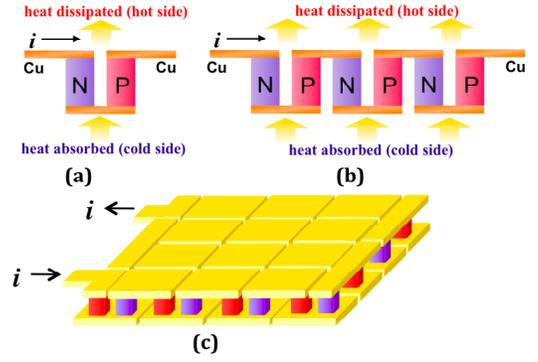


Figure 1. (a) The side view of a single TEC device (b) multiple TEC devices connected electrically in series and thermally in parallel (c) the 3D view of a 4x4 array of thin-film TEC devices.

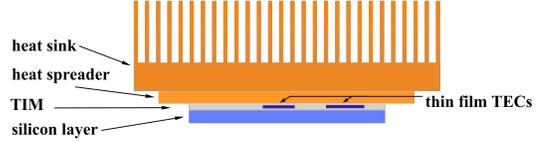


Figure 2. Integration of the thin-film TECs into the chip package.

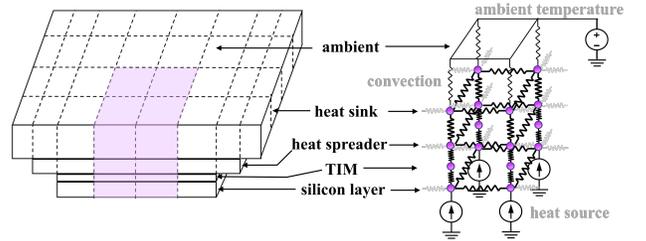


Figure 3. Compact thermal model of the chip package.

[13]:

$$q_c = \alpha i \theta_c - \frac{1}{2} r i^2 - k(\theta_h - \theta_c) \quad (1)$$

$$q_h = \alpha i \theta_h + \frac{1}{2} r i^2 - k(\theta_h - \theta_c) \quad (2)$$

where i is the electrical supply current of the TEC device; α is the Seebeck coefficient of the TEC device; r and κ are the electrical resistance and thermal conductance of the device, respectively. The first term in these two equations describes the Peltier cooling effect. The second term is due to Joule heating that occurs in the TEC device – half of the Joule heat is dissipated at the cold side and the other half at the hot side. The third term is contributed by heat conductance from the hot side to the cold side.

According to Equations (1) and (2), the input power of a TEC device is equal to

$$p_{TEC} = q_h - q_c = r i^2 + \alpha i \cdot \Delta\theta \quad (3)$$

In steady state, the input power of the TEC devices will be converted to heat in the chip package before being dissipated to the ambient. Hence, an excessive deployment of TEC devices and/or improper setting of the TEC supply current levels could lead to the overheating of the chip package.

It is worth to note that although the above equations are widely used in the literature, they have omitted the Thomson effect, which accompanies with the Peltier effect [14]. The Thomson effect is caused by the dependence of the Seebeck coefficient on temperature. However, the Thomson effect can be accounted for by substituting α with $(\alpha_H + \alpha_C)/2$, where α_H

and α_C are the Seebeck coefficients at the highest and lowest allowable operating temperature of the system, respectively [14]. In our model, we have adopted this more accurate approximation.

In order to enhance the cooling effect, multiple TEC devices can be connected electrically in series and thermally in parallel (Figure 1(b)). Figure 1(c) shows the 3D view of a 4×4 array of super-lattice thin-film TEC devices [1]. Thin-film TEC devices occupy small areas. For instance, a 7×7 array of thin-film TEC devices has a lateral dimension of about $3.5 \text{ mm} \times 3.5 \text{ mm}$ [1]. Hence, the lateral area of a single TEC device can be estimated by $0.5 \text{ mm} \times 0.5 \text{ mm}$.

B. Thin-film Thermoelectrics based Active Cooling System

Figure 2 illustrates the integration of the thin-film TEC devices into the chip package [1]. The thin-film TEC devices are immersed in the thermal interface materials (TIM) layer, lying between the silicon layer and the heat spreader layer.

The supply current of the on-chip TEC devices is provided by an external source via one or multiple pins. In this paper, we focus the simplest setting where only one extra pin is added to the chip package. As a result, we assume that the supply current of all the on-chip TEC devices are the same. Allowing only one extra pin is desirable to the high performance microprocessor systems for which the thin-film TEC technology is intended. These chips are already restricted in pin usage (a maximum number of pins would be desirably allocated for I/O etc.) and have limited room for extra pins.

The deployment and the supply current levels of the TEC devices need to be carefully determined to prevent the chip package from overheating. We will provide the formal definition of the cooling system optimization problem in Section V. Before that, we first present our compact thermal model for chip packages with integrated TEC devices in Section IV.

IV. COMPACT THERMAL MODEL FOR CHIP PACKAGE WITH ON-CHIP THERMOELECTRIC COOLERS

As a design requirement, the cooling system should guarantee that the peak *steady state* temperature of the silicon layer stays below the maximum allowable temperature under the worst-case power profile. The compact thermal model derived in this section is intended for the steady state analysis of the chip package.

A. Compact Thermal Model for the Chip Package

There is a well-known duality between heat transfer and electrical phenomena. The heat flow can be treated as “current” passing through thermal conductance, creating temperature differences analogous to “voltage” drops. Such equivalency has been leveraged to develop *compact thermal models* for chip packages [7]. Figure 2 demonstrates the typical chip package for high-performance microprocessors. The silicon layer is placed against a heat spreader layer, made of aluminum or copper, with a TIM layer in between. The heat spreader layer is in turn placed against a heat sink cooled by a fan [7].

In order to derive a compact thermal model for the chip package, each layer is first dissected into smaller tiles. Next, a thermal conductance network can be constructed, where each node corresponds to a tile and each edge represents the thermal conductance between adjacent tiles. Air convection is described by a thermal conductor between the nodes in the heat sink layer and the ambient node. The ambient temperature can be modeled by a constant voltage between the ambient node and the hypothetical ground node representing the absolute zero temperature. Power dissipation in the silicon layer is modeled as current sources. The left part of Figure 3 demonstrates the dissection of the layers into tiles, while the right part depicts the conductance network for the shaded portion of the package. Notice that the thermal capacitance is not included in our model since we are focusing on the steady state behavior of the package.

Validation of existing architecture-level thermal simulation tools based on this model has shown that the compact model achieves excellent agreement with the accurate finite element models [7, 15].

B. Compact Thermal Model for Systems with TECs

We propose a thermal model for the TEC device based on Equation (1) and (2) as depicted in Figure 4. The two nodes represent the hot side and the cold side of the device. A thermal conductor κ connecting the two nodes models the term $\kappa(\theta_h - \theta_c)$ in Equation (1) and (2). The Joule heating effect can be described by two heat sources connected to the hot side and cold side node, each having the magnitude of $ri^2/2$. The Peltier heat $ai\theta_c$ absorbed at the cold side can be described by a thermal conductor ai connecting the cold side and the ground node which represents the absolute zero temperature. Likewise, the Peltier heat $ai\theta_h$ released at the hot side can be modeled by a negative thermal conductor $-ai$ connecting the hot side and the ground. We note that the values of these two conductors depends on the supply current. Hence, in Figure 4, arrows were used to indicate that they are “tunable conductors”. In addition, we place two thermal conductors g_h and g_c at the hot/cold nodes to account for the contact thermal resistance between the hot/cold side and the rest of the package. Such thermal conductors which lie between the hot side and the ambient end up playing an important role in the thermal runaway problem. We remind the reader that Figure 4 represents a thermal flow circuit and the physical current i does not flow through any of these “conductances”.

As mentioned above, the TEC devices reside in the TIM layer. After the set of silicon tiles that need to be covered by TEC devices is determined, we simply substitute the corresponding TIM node with the thermal model of the TEC device. We note that after the substitution, at a fixed value of TEC supply current, *the compact thermal model for the package is still a linear network*. Hence, standard linear

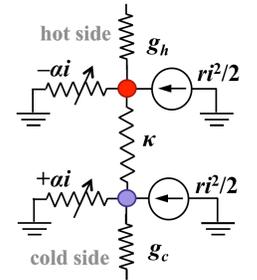


Figure 4. TEC device thermal model.

network analysis techniques can be applied to study the thermal behavior of the package.

C. Thermal Steady State Analysis

The thermal steady state of the network can be computed using the nodal analysis technique [16]. Let us use notations SIL , HOT , and CLD to denote the set of nodes in the silicon layer, the hot side, and the cold side of the TEC devices, respectively. We use a vector \mathbf{p} to represent the input heat power at each node, where p_k equals the heating power of the transistors inside the silicon tile if $k \in SIL$, $ri^2/2$ if $k \in HOT \cup CLD$, and 0 otherwise. Then, the steady state temperature profile $\boldsymbol{\theta}$ is related to the power profile \mathbf{p} by a system of linear equations

$$(\mathbf{G} - \mathbf{D})\boldsymbol{\theta} = \mathbf{p} \quad (4)$$

where matrices \mathbf{G} and \mathbf{D} are defined in the following

$$\mathbf{G} = \begin{pmatrix} \sum_{0 \leq l \leq n} g_{1l} & -g_{12} & \dots & -g_{1n} \\ \dots & \dots & \dots & \dots \\ -g_{k1} & \dots & \sum_{0 \leq l \leq n} g_{kl} & \dots -g_{kn} \\ \dots & \dots & \dots & \dots \\ -g_{n1} & -g_{n2} & \dots & \sum_{0 \leq l \leq n} g_{nl} \end{pmatrix} \quad \mathbf{D} = \begin{pmatrix} \alpha_1 & 0 & \dots & 0 \\ & \alpha_2 & \dots & 0 \\ & & \alpha_k & \\ & 0 & \dots & \dots \\ 0 & \dots & 0 & \alpha_n \end{pmatrix} \quad (5)$$

Here g_{kl} is the thermal conductance between node k and node l (g_{kl} is zero if node k and node l are not adjacent in the network); α_k equals to $+\alpha$ if $k \in HOT$, $-\alpha$ if $k \in CLD$, and 0 otherwise, and α accounts for the transfer of Peltier heat in the network.

Matrix \mathbf{G} has several special structural properties essential to our proposed active cooling system optimization algorithm. They are captured by the following definitions and Theorem 1. For the sake of brevity, theorem 1 and several theorems in Section V are stated without proofs. The formal proofs are provided in Appendix A.

Definition 1: We call a network an *irreducible network* if and only it contains at least one path between any given pair of nodes.

Given an $n \times n$ symmetric matrix $\mathbf{M} = (m_{ij})_{n \times n}$, we can construct a corresponding network containing n nodes. We connect the i^{th} and j^{th} node by an undirected edge if $m_{ij} \neq 0$.

Definition 2: A matrix is called an *irreducible matrix* if and only if its corresponding network is an irreducible network.

Definition 3: An $n \times n$ real matrix \mathbf{M} is *positive definite* if $\mathbf{x}^T \mathbf{M} \mathbf{x} > 0$ for all non-zero vectors \mathbf{x} with real elements.

Definition 4: A *Stieltjes matrix* is a real symmetric matrix with non-positive off-diagonal elements [11].

Theorem 1: The matrix \mathbf{G} defined in Expression (5) is an irreducible positive definite Stieltjes matrix.

V. OPTIMIZATION OF THE ACTIVE COOLING SYSTEM

A. Problem Definition

Based on the discussions in Sections III and IV, we define

active cooling system configuration problems as follows.

Problem 1 (Cooling System Configuration): Given: 1) $p \times q$ tiles representing the silicon layer where each tile has the same area as a TEC device, and 2) the worst case power consumption of each tile;

Determine: 1) the minimal set of tiles that needs to be covered by the TEC devices, and 2) the proper supply current of the TEC devices;

Objective: the peak steady state temperature of the silicon layer does not exceed the maximal allowable temperature.

B. Optimization Algorithms

Figure 5 provides the pseudo code of our algorithm, which solves the deployment problem following the greedy strategy. It works in an iterative manner. In the beginning, it identifies the set of tiles T whose temperature exceeds the maximum allowable operating temperature θ_{max} and covers these tiles with TEC devices (Line 4, 7). Then, a subroutine will be invoked to compute the supply current of the TEC devices that minimizes the peak temperature of the tiles in the silicon layer for the given TEC deployment (Line 8). We will elaborate on this subroutine in the subsequent section. Adding more TEC devices into the package has two consequences: The temperatures of the tiles that are covered by these TEC devices may decrease; however, the temperatures of other tiles might increase since the new set of TEC devices dissipate an extra amount of heat in the package. Hence, in each iteration, after adding TEC devices, we update set T (Line 10). If T is an empty set, the peak tile temperature must be below θ_{max} . The algorithm then returns true, indicating a proper deployment is found (Line 11~12). If all the tiles whose temperature are above θ_{max} have already been covered by the TEC devices, the algorithm returns false, indicating that it failed to find a proper TEC deployment (Line 13~14). Otherwise, the main loop proceeds to its next iteration.

1) The peak tile temperature minimization problem

This section would elaborate on the subroutine for peak tile temperature minimization (invoked in the 8th line of Figure 5).

Problem 2 (Peak tile temperature minimization): Given the deployment of the TEC devices, determine the supply current

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ALGORITHM GreedyDeploy(p)
INPUT: p // the worst case power consumption of each tile
OUTPUT:  $S_{TEC}$  // the set of tiles that need TEC devices
1 BEGIN
2    $S_{TEC} = \Phi$ ;
3   Solve  $\mathbf{G}\boldsymbol{\theta} = \mathbf{p}$ ;
4    $T = \{tile_k \mid tile_k.temperature > \theta_{max}\}$ ;
5
6   WHILE (True) BEGIN
7      $S_{TEC} = S_{TEC} \cup T$ ;
8     Find  $i_{opt}$ , which minimizes the peak tile temperature;
9     Solve  $(\mathbf{G} - i_{opt}\mathbf{D})\boldsymbol{\theta} = \mathbf{p}$ ;
10     $T = \{tile_k \mid tile_k.temperature > \theta_{max}\}$ ;
11    IF ( $T == \Phi$ )
12      RETURN True;
13    IF ( $T \subseteq S_{TEC}$ )
14      RETURN False;
15  END
16 END

```

Figure 5. The greedy algorithm for the deployment problem.

of the TEC devices which minimizes the maximum temperature of the tiles.

This problem can be formulated as follows:

$$\text{minimize } \max\{\theta_k(i) \mid \forall k \in SIL\} \quad (6)$$

$$\text{subject to } (\mathbf{G} - i\mathbf{D})\boldsymbol{\theta} = \mathbf{p}, i \geq 0 \quad (7)$$

In the following, we will develop a convex programming based algorithm for this problem. Firstly, we show that there exists an upper limit λ for the supply current of the TEC devices. Any supply current level larger than λ would cause thermal runaway. Mathematically, as the supply current approaches λ , the temperature of each tile approaches infinity. We provide a polynomial time algorithm to calculate λ . Then, we propose a conjecture in matrix theory. Based on the conjecture, we provide a sufficient condition for the cost function (6) to be a convex function of the supply current i over $[0, \lambda)$.

2) The active cooling system thermal runaway phenomenon

We will leverage the theory of inverse-positive matrix [11] to show the existence of the upper limit λ in this section.

Theorem 2: Given a positive definite irreducible Stieltjes matrix \mathbf{G} and a real diagonal matrix \mathbf{D} with at least one positive element, define

$$\lambda = \inf \left\{ \frac{\boldsymbol{\theta}^T \mathbf{G} \boldsymbol{\theta}}{\boldsymbol{\theta}^T \mathbf{D} \boldsymbol{\theta}} \mid \boldsymbol{\theta}^T \mathbf{D} \boldsymbol{\theta} > 0 \right\}$$

Let $\mathbf{A} = \mathbf{G} - i\mathbf{D}$. We have the following:

- 1) For any $i \in [0, \lambda)$, \mathbf{A} is positive definite.
- 2) When $i = \lambda$, \mathbf{A} is singular and semidefinite.
- 3) For any $i \in [\lambda, +\infty)$, \mathbf{A} is not positive definite.

Theorem 3: Given matrix \mathbf{A} and real number λ as defined in Theorem 2 and denoting $\mathbf{H} = \mathbf{A}^{-1}$, for any $1 \leq k, l \leq n$, we have

$$\lim_{i \rightarrow \lambda^-} h_{kl}(i) = +\infty \quad (8)$$

where symbol $h_{kl}(i)$ represents the element of \mathbf{H} in the k^{th} row and the l^{th} column (as a function of i).

Figure 6 depicts $h_{kl}(i)$ as a function of i . Note that according to Equation (4), $\boldsymbol{\theta} = \mathbf{A}^{-1} \cdot \mathbf{p} = \mathbf{H} \cdot \mathbf{p}$. Thus, the physical interpretation of h_{kl} is the temperature of node k if a unit of power is input at node l . Theorem 2 reveals that if there is one node in the network that has non-zero input power, then, as i approaches λ , the temperature of each node approaches infinity, indicating thermal runaway.

The physical interpretation of the thermal runaway is as follows. λ represents the input current level which causes the active cooling system to have zero heat pumping capability since Peltier cooling is offset by ohmic heating and heat conduction. In the thermoelectric literature, this occurs when the coefficient of performance of the thermoelectric cooler becomes zero [17]. Similar situations have been investigated but under different boundary conditions [17]. The above

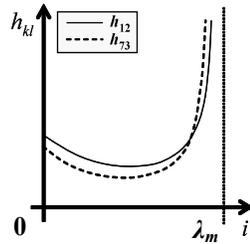


Figure 6. $h_{kl}(i)$ as functions of the supply current i .

discussion reveals we should restrict the search of the current level that minimizes the maximum silicon layer temperature within $[0, \lambda)$.

This upper limit λ can be calculated using a binary search based on Theorem 1. Cholesky decomposition ($O(n^3)$ time complexity) is employed to check whether a matrix is positive definite [18].

3) The convexity of the cost function

In this section, based on a conjecture, we provide a sufficient condition for the maximum temperature of the tiles to be a convex function of i over $[0, \lambda)$.

Definition 5: Given a vector \mathbf{r} , denote the k^{th} element of \mathbf{r} by r_k . We define notation $\text{DIAG}(\mathbf{r})$ to be a square diagonal matrix with all off-diagonal elements being zero and the diagonal element in the k^{th} row and k^{th} column equals to r_k .

Conjecture 1: Given an $n \times n$ positive definite Stieltjes matrix \mathbf{S} , denote $\mathbf{R} = \mathbf{S}^{-1}$. Denoting the k^{th} and l^{th} row vector of \mathbf{R} by \mathbf{r}_k and \mathbf{r}_l , then $\text{DIAG}(\mathbf{r}_k) \cdot \mathbf{R} \cdot \text{DIAG}(\mathbf{r}_l)$ is positive definite for any $1 \leq k, l \leq n$.

Although we have not yet been able to prove this conjecture theoretically, we have randomly generated millions of positive definite Stieltjes matrices and verified this property in all cases. Hence, it seems that this property is applicable in all practical cases.

Theorem 4: Given matrix \mathbf{H} and real number λ as defined in Theorem 2, if Conjecture 1 holds true, then every element $h_{kl}(i)$ of matrix \mathbf{H} is a convex function of supply current i over $[0, \lambda)$.

Theorem 3 and Theorem 4 characterize $h_{kl}(i)$ over range $[0, \lambda)$: it is a nonnegative convex function which approaches $+\infty$ when i approaches λ . Figure 6 illustrates these properties.

According to Equation (4), $\boldsymbol{\theta} = \mathbf{A}^{-1} \cdot \mathbf{p} = \mathbf{H} \cdot \mathbf{p}$. Hence, the temperature of the k^{th} node in the network equals

$$\theta_k(i) = \frac{1}{2} ri^2 \sum_{i \in \text{HOT} \cup \text{CLD}} h_{kl}(i) + \sum_{i \in \text{SIL}} (h_{kl}(i) \cdot p_i) = \frac{1}{2} ri^2 \cdot \eta(i) + \zeta(i) \quad (10)$$

We note that if Conjecture 1 is true, functions $\eta(i)$ and $\zeta(i)$ are both convex functions of i since they are positive weighted sums of convex functions. However, the product term $ri^2\eta(i)/2$ is not guaranteed to be a convex function in general. In the following, we derive a simple sufficient condition to check whether $\theta_k(i)$ is a convex function. The verification of the sufficient condition can be performed in polynomial time. According to Equation (10), we have

$$\begin{aligned} \theta_k''(i) &= r\eta(i) + ri\eta'(i) + \frac{1}{2}ri^2\eta''(i) + \zeta''(i) \\ &\geq r\eta(i) + r\eta'(i) \cdot i \end{aligned} \quad (11)$$

Noticing that $\eta'(i)$ is an increasing function since $\eta(i)$ is convex, we have the following sufficient condition:

Theorem 5: Assuming Conjecture 1 holds, if the following problem (12) is infeasible, then $\theta_k(i)$ is convex over $[i_t, i_{t+1}]$. Here, i_t and i_{t+1} are real values satisfying $0 \leq i_t < i_{t+1} < \lambda$.

$$r\eta(i) + r\eta'(i_t) \cdot i < 0, i \in [i_t, i_{t+1}] \quad (12)$$

In the above formulation, $\eta'(i_t)$ is a constant that equals to the derivative of $\eta(i)$ at i_t . The left hand side of the inequality

is a convex function, since it is the sum of a convex function and a linear function. Hence, problem (12) is a convex feasibility problem, which can be solved in polynomial time.

In order to calculate $\eta'(i)$, we note that $d\mathbf{H} / di = \mathbf{HDH}$. Since

$$\eta'(i) = \sum_{I \in \text{HOT} \cup \text{CLD}} h_{kl}'(i) \quad (13)$$

$\eta'(i)$ can be determined accordingly in polynomial time.

We note that $\theta_k(i)$ is twice differentiable over $[0, \lambda)$. Hence, the convexity of the function over each of the sub-ranges implies the convexity of the function over $[0, \lambda)$. We thus reach the following theorem which enables us to check whether $\theta_k(i)$ is convex over $[0, \lambda)$ in polynomial time.

Theorem 6: Assuming Conjecture 1 holds, given any finite sequence of real numbers satisfying $0 = i_0 < \dots < i_t < i_{t+1} < \dots < i_m = \lambda$, if convex feasibility problem (12) is infeasible for each $[i_t, i_{t+1}]$, then $\theta_k(i)$ is convex over $[0, \lambda)$.

In theorem 6, the increasing sequence $\{i_t\}$ can be chosen arbitrarily. For instance, we can chose $0 = i_0 < i_1 = \lambda$. This would minimize the runtime of the checking process. However, the optimality check would be quite pessimistic since $\eta'(0)$ is a very loose lower bound for $\eta'(i)$ over $[0, \lambda)$. Dividing $[0, \lambda)$ into more sub-ranges would increase the accuracy of the lower bound for $\eta'(i)$ at the expense of runtime.

4) Algorithm minimizing the peak tile temperature

Based on the above discussions, we developed a convex programming based algorithm for Problem 2. In the beginning, we determine the upper limit λ . Then, we employ the gradient descent method to solve formulation (6~7) [18]. At the end, we perform an additional optimality check based on Theorem 4. If Conjecture 1 is true and the problem instance passes the optimality check, then, formulation (6~7) is a convex optimization problem. Thus, the solution obtained by the gradient descent method is guaranteed to be optimal.

VI. EXPERIMENTAL RESULTS

We have implemented our optimization framework in C++ and evaluated our proposed algorithms on various benchmarks. All the experiments were carried out on a Linux server with four 2.8 GHz Intel® Xeon™ processors and 1 GB memory. In our implementation, the physical parameters (Seebeck coefficient, electrical resistivity and thermal conductivity) of the thin-film TEC device provided by Chowdhury *et al.* [1] are used. Other parameters such as the silicon thermal conductivity, convection, etc., were set according to an existing thermal simulator, HotSpot 4.1 [7]. We have first validated our thermal model against HotSpot 4.1 by performing steady state analysis without the TEC devices. For a given floorplan and a set of power traces, we performed steady state analysis using both our model and Hotspot 4.1 and compared the temperature of each tile generated by them. The two results agreed closely – the worst-case difference is less than 1.5 °C. Next, we conducted experiments with our model including the TEC devices to evaluate the impact of the active cooling system on the thermal behavior of the chip package.

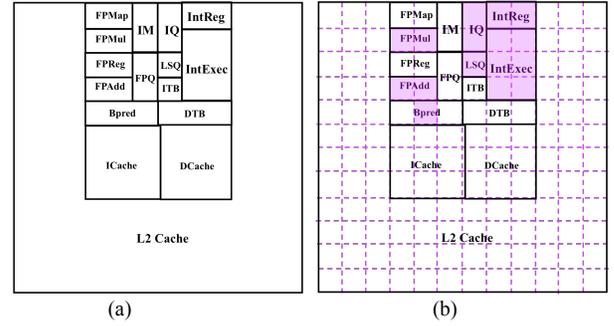


Figure 7. (a) The floorplan of an Alpha-21364-like microprocessor (b) dividing the floorplan into 12x12 tiles.

A. Experimental Study for a DEC Alpha-21364-Like Chip

Our first set of experiments was performed on a microprocessor floorplan similar to that of a 65nm DEC Alpha-21364 microprocessor (Figure 7(a)) [7]. The silicon die has a dimension of 6 mm x 6 mm. As mentioned in Section III.A, we estimated the lateral area of a single TEC device by 0.5 mm x 0.5 mm. Hence, the silicon die was divided into 12x12 tiles in our experiment (Figure 7(b)). To obtain the worst case power consumption of each silicon tile, we simulated the SPEC2000 benchmark suite [19] using M5 simulator [20] with an embedded architecture level power simulator Wattach [21]. We collected the worst case power consumption of each functional unit and added a 20% margin to them. Based on these numbers, we calculated the worst case power consumption of each tile. As mentioned earlier, the power dissipation of the functional units is highly uneven. The power density of the heavily used units such as integer register (IntReg) can be as high as 282.4 W·cm⁻² while that of L2 Cache is only 25.0 W·cm⁻². The total worst case power consumption of the chip is 20.6 W. The heavily used units such as integer register, integer execution unit (IntExec), instruction queue (IQ), load and store queue (LSQ), floating point multiplier (FPMul), and floating point adder (FPAdd) consumes 28.1% of the total power while occupying only 10.4% of the total area.

The first row of Table I summarizes our experimental results on the Alpha-21364 microprocessor floorplan. We first computed the steady state of the Alpha-21364 chip without the TEC devices. The temperature of the hottest tile in the silicon layer is given in Column θ_{peak} (91.8 °C). Next, we employed our GreedyDeploy algorithm to determine the set of tiles that

TABLE I. EXPERIMENTAL RESULTS FOR THE BENCHMARKS

	No TEC	Greedy Deployment				Full Cover	
	θ_{peak} °C	#TECs	θ_{limit} °C	I_{opt} A	P_{TEC} W	$\min\theta_{peak}$ °C	SwingLoss °C
Alpha	91.8	16	85	6.10	1.31	90.2	5.2
HC01	90.1	12	85	6.82	1.26	88.5	3.5
HC02	92.5	15	85	6.90	1.63	90.9	5.9
HC03	89.8	16	85	7.24	1.93	88.3	3.3
HC04	90.5	16	85	6.57	1.57	88.9	3.9
HC05	89.9	18	85	7.10	2.09	88.4	3.4
HC06	94.2	17	89	5.27	1.03	92.6	3.6
HC07	91.2	14	85	8.26	2.24	89.6	4.6
HC08	89.4	11	85	5.05	0.60	87.9	2.9
HC09	95.3	12	88	10.42	3.02	93.8	5.8
HC10	90.6	14	85	7.82	1.97	89.1	4.1
Avg.					1.70		4.2

need to be covered by TEC devices. The maximum allowable tile temperature was set to 85 °C (Column θ_{limit}). The GreedyDeploy algorithm determined 16 tiles that need to be covered by TEC devices (Column #TECs). These tiles are shaded in Figure 7(b). It can be seen that only the functional units with high power density (such as IntReg and IntExec) are needed to be covered. Table I also reports the supply current (Column I_{opt}) determined by the GreedyDeploy algorithm, as well as the power consumption of the TEC devices (Column P_{TEC}). The external power consumed by the TEC devices is reasonably small (1.31 W). Our algorithm is efficient in terms of execution time – the deployment and level configuration algorithms combined terminated within 2 minutes.

We compared our optimization framework with a baseline strategy where every tile is covered by a TEC device with the supply current determined by our convex-programming based peak tile temperature minimization algorithm (Section V.C). The experimental results are listed in the two columns under the Full Cover label. It is noticeable that at the optimal supply current, the peak tile temperature is as high as 90.2 °C (Column $\min\theta_{peak}$), 5.2 °C higher (Column SwingLoss) than what could be achieved by our GreedyDeploy algorithm. As mentioned in Section III.B, the external power consumed by the TEC devices would counteract their cooling effect. This phenomenon reveals that placing excessive TEC devices would decrease the efficiency of the active cooling system.

B. Experimental Study for Hypothetical Chips

The second set of experiments was conducted on 10 hypothetical chips, each represented by a 12x12 array of tiles corresponding to a 6 mm x 6 mm floorplan. For each chip, we first randomly divided the floorplan into several functional units, each containing between 5 and 15 tiles. In order to imitate the non-uniform power distribution, we randomly selected two units and assigned them higher power density than the rest. Typically, the two selected units consume 30% of chip power while occupying 10% of the chip area. The total power consumption of the chip ranges from 15 W to 25 W.

We conducted experiments and a comparison similar to those described in Section VI.A. Rows 2 until 11 of Table I provide the experimental results. We observe that for all the benchmark chips except for HC06 and HC09, the GreedyDeploy algorithm was able to guarantee that the maximum tile temperatures stay below the given limit (85 °C) with reasonably small power overhead (around 2 W). Without the TEC devices, the maximum tile temperature can be as high as 92.5 °C (HC02). Hence, the active cooling swing can reach 7.5 °C. Here the term “cooling swing” refers to the drop of the maximum tile temperature after employing the active cooling system. This conforms to the maximum on-demand cooling swing (5.4 °C to 9.6 °C) reported by Chowdhury *et al.* [1]. Besides, for each benchmark, the execution time of our algorithms is less than 3 minutes.

For benchmark chips HC06 and HC09, our algorithms fail when the maximum allowable temperature is set to 85 °C. This is mainly because the temperatures of the hot spots in these

two chips are too high (Column 1). It is beyond the capability of the TEC devices to cool them down to 85 °C. However, when the maximum allowable temperature is set to higher values (89 °C for HC06 and 88 °C for HC09, Column 3), our algorithm would be able to determine proper deployments and supply currents for these two benchmarks.

Finally, similar to the Alpha 21364 case, for these ten benchmark chips, assigning a TEC device to every tile increases the lowest achievable peak tile temperature. Compared to the deployment determined by the GreedyDeploy algorithm, the cooling swing loss is 4.2 °C on average. This confirms our conclusion that allocating excessive TEC devices would reduce the overall efficiency of the active cooling system and the system design process benefits from a systematic approach to this problem.

VII. CONCLUSIONS

In this paper, we have examined the design and optimization of an on-chip active cooling system based on thin-film thermoelectric coolers. We first established the compact thermal model for the chip package with integrated thin-film TEC devices. Next, we formulated the configuration problem of active cooling system. We proposed algorithms for both problems and discussed the optimality condition of the algorithms. For most of the benchmarks, our algorithms were able to determine the proper deployment and supply current of the TEC devices which guarantee that under the worst-case power consumption, the chip stays below the given limit of 85 °C, commonly used in practice. Moreover, for all benchmarks, the execution time of our algorithm is less than 3 minutes.

APPENDIX A. THEORETICAL FOUNDATION FOR THE ANALYSIS OF ON-CHIP THERMOELECTRIC COOLING SYSTEMS

In Appendix A, we build up the theoretical foundation for the analysis of the on-chip thermoelectric cooling systems upon the theory of inverse-positive matrix [11]. The theorems stated without proofs in the previous sections are formally proven for a generalized network. The thermal network of the chip package with integrated TEC devices is a special case of the generalized network. Although inverse-positive matrix has been studied extensively in the literature [11], to the best of our knowledge, none of them has considered the inclusion of tunable negative conductors, which play a critical role in the analysis of the thermoelectric cooling system. We note that due to the generalization, the theorems presented the appendix might be stated slightly different than the corresponding theorems in the previous sections.

The generalized network under consideration is a connected conductor network containing both fixed and tunable conductors (Figure 8(a)). The fixed conductors must have positive values. In Figure 8, the conductors colored in black are the fixed conductors. We require these fixed conductors to form a connected sub-network. A special node labeled 0 in this sub-network is defined as the ground node. The tunable conductors can be placed between any node in this sub-network and the ground node. In Figure 8(a), they are colored

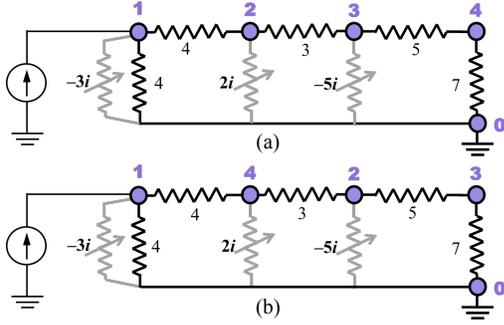


Figure 8. A simple example of the generalized network (a) label the nodes such that the corresponding matrix \mathbf{G} is a fully irreducible matrix (b) label the nodes such that the corresponding matrix \mathbf{G} is not a fully irreducible matrix.

in gray and attached with arrows. The value of the tunable conductor connected to the k^{th} node is $-\alpha_k i$, where i is a real number representing an external tuning force (in the case of thermoelectric cooling system, i is the supply current). All the tunable conductors share the same value of i . The tunable conductors can have either positive or negative values. Further, in order to make our analysis to be applicable to the thermoelectric cooling system, we at least one of tunable conductor has negative value. That is, at least one α_k has to be positive. This is due to the fact that a TEC device would introduce a negative tunable thermal conductor to the thermal model of the chip package.

Let us denote the fixed conductance between node k and node l is denoted by g_{kl} . We construct matrices \mathbf{G} and \mathbf{D} to describe the sub-network formed by the fixed and tunable conductors, respectively. The definitions of matrices \mathbf{G} and \mathbf{D} are given in Expression (A1).

$$\mathbf{G} = \begin{pmatrix} \sum_{0 \leq l \leq n} g_{1l} & -g_{12} & \cdots & -g_{1n} \\ \cdots & \cdots & \cdots & \cdots \\ -g_{k1} & \cdots & \sum_{0 \leq l \leq n} g_{kl} & \cdots -g_{kn} \\ \cdots & \cdots & \cdots & \cdots \\ -g_{n1} & -g_{n2} & \cdots & \sum_{0 \leq l \leq n} g_{nl} \end{pmatrix} \quad \mathbf{D} = \begin{pmatrix} \alpha_1 & 0 & \cdots & 0 \\ \alpha_2 & \cdots & 0 & \\ \alpha_k & \cdots & \cdots & \\ 0 & \cdots & \cdots & \\ 0 & \cdots & 0 & \alpha_n \end{pmatrix} \quad (\text{A1})$$

Definition 6: Given an $n \times n$ irreducible matrix, if for each $k = 1, 2, \dots, n$, the sub-matrix formed by its first k row and k column is irreducible, then we call the given matrix a *fully irreducible* matrix.

Lemma 1: Given a generalized conductor network containing at least one negative conductor, it is always possible to label the nodes such that 1) matrix \mathbf{G} is fully irreducible, and 2) α_1 , the element at the upper-left corner of matrix \mathbf{D} is positive. The definitions of matrices \mathbf{G} and \mathbf{D} are given by Expression (5).

Proof: Since the chip package containing at least one TEC devices, its thermal model contains at least one negative thermal conductor. Let us label the non-ground end node of a negative conductor as the first node, the element at the upper-left corner of matrix \mathbf{D} would be positive. Starting from this node, we continue to label the nodes such that the latest labeled node is adjacent to at least one of the nodes that have

been labeled. This labeling order ensures that the sub-matrix formed by the first k row and k column of \mathbf{G} corresponds to a connected component. Hence, \mathbf{G} is fully irreducible. ■

For instance, the labeling in Figure 8(a) leads to fully irreducible matrix \mathbf{G} , while the labeling in Figure 8(b) does not. Without loss of generality, in the following, we assume that the network modeling the chip package is properly labeled such that matrix \mathbf{G} is fully irreducible, and the element at the upper-left corner of matrix \mathbf{D} is positive.

Notations: the notations in Appendix A are fixed as follows unless stated explicitly:

n : The total number of nodes (except for the ground node) in the networks.

\mathbf{G} : A matrix as defined in Expression (A1).

\mathbf{D} : A matrix as defined in Expression (A1).

\mathbf{A} : An $n \times n$ matrix defined as $\mathbf{G} - i\mathbf{D}$. Here i is a real number. Note that \mathbf{A} is a function of i (a mapping from a scalar to a matrix).

\mathbf{H} : The inverse of matrix \mathbf{A} , i.e., $\mathbf{H} = \mathbf{A}^{-1}$. Similar to matrix \mathbf{A} , matrix \mathbf{H} is also a function of i .

\mathbf{A}_k : Sub-matrix of \mathbf{A} formed by the common parts of the first k row and first k column of \mathbf{A} . As a special case, \mathbf{A} is identical to \mathbf{A}_n . Notations \mathbf{G}_k and \mathbf{D}_k are defined in a similar way.

\mathbf{A}_{kl} : Modified matrix \mathbf{A} after k^{th} row and l^{th} column removed.

Vector Comparison Notations: Given a vector \mathbf{v} , we write $\mathbf{v} \geq \mathbf{0}$ if and only if each element of \mathbf{v} is nonnegative. We write $\mathbf{v} > \mathbf{0}$ if and only if each element of \mathbf{v} is nonnegative and \mathbf{v} contains at least one positive element. We write $\mathbf{v} \gg \mathbf{0}$ if and only if each element of \mathbf{v} is positive.

Theorem 1: Matrix \mathbf{G} is a fully irreducible positive definite Stieltjes matrix.

Proof: We have mentioned in our earlier discussion that \mathbf{G} is fully irreducible. Secondly, It is easy to verify that \mathbf{G} is a Stieltjes matrix according to Definition 3. Finally, it is known that matrix \mathbf{G} is a positive definite matrix [22]. ■

Lemma 2: If vector $\boldsymbol{\theta}$ satisfies $\mathbf{G}\boldsymbol{\theta} > \mathbf{0}$, then $\boldsymbol{\theta} \gg \mathbf{0}$.

Proof. Let us assume $\mathbf{G}\boldsymbol{\theta} = \mathbf{u} > \mathbf{0}$. Let us prove $\boldsymbol{\theta} \gg \mathbf{0}$ by contradiction.

Firstly, it is known that the inverse of a positive definite Stieltjes matrix (either reducible or irreducible) contain only nonnegative elements [11]. Hence, we have $\boldsymbol{\theta} \geq \mathbf{0}$. Suppose the l^{th} element θ_l of $\boldsymbol{\theta}$ is zero, the l^{th} equation of $\mathbf{G}\boldsymbol{\theta} = \mathbf{u}$ can be written as

$$\sum_{j \in Nr(l)} g_{lj} (\theta_l - \theta_j) + g_{ll} \cdot \theta_l = u_l$$

where $Nr(l)$ is the set of neighboring nodes of node l , and u_l is the l^{th} element of vector \mathbf{u} . Obviously, $u_l \geq 0$. Since the coefficients $g_{ij} > 0$, if θ_l is zero, each θ_j must be non-positive. As mentioned above, θ_j cannot be negative. Hence, each of them must be zero. Repeat this reasoning, we can prove that if θ_l is zero, the θ value of any node in the connected component containing node l must be zero. Further, we note that since \mathbf{G} is an irreducible matrix, every node should belong to a

connected component. Hence, $\boldsymbol{\theta} = \mathbf{0}$, and thus $\mathbf{G}\boldsymbol{\theta} = \mathbf{0}$. However, this is contracted to $\mathbf{u} > \mathbf{0}$. Therefore, every element of $\boldsymbol{\theta}$ must positive. ■

Lemma 3: Every element of the inverse of a fully irreducible positive definite Stieltjes matrix must be positive.

Proof: Let us use \mathbf{u}_k to denote a vector whose k^{th} element is one and other elements are zeros. We note that $\mathbf{G} \cdot \mathbf{G}^{-1} = \mathbf{I} = (\mathbf{u}_1, \mathbf{u}_2, \dots, \mathbf{u}_n)$. Besides, $\mathbf{u}_k > \mathbf{0}$ for each $k = 1, 2, \dots, n$. According to Lemma 2, each element of \mathbf{G}^{-1} must be a positive number. ■

Lemma 4: For every $k \leq n$, \mathbf{G}_k is an irreducible positive definite Stieltjes matrix.

Proof: Firstly, since \mathbf{G} is fully irreducible, \mathbf{G}_k must be irreducible. Secondly, since \mathbf{G} is symmetric and positive definite, $\det(\mathbf{G}_k) > 0$ for $k = 1, 2, \dots, n$. Hence, \mathbf{G}_k must be positive definite. Finally, it is easy to verify that \mathbf{G}_k is a Stieltjes matrix. ■

Lemma 5: For any $k \leq n$, $\det(\mathbf{A}_k) = 0$ has at least one positive root. Moreover, denote the smallest positive root of equation $\det(\mathbf{A}_k) = 0$ as λ_k , we have

$$\lambda_n < \lambda_{n-1} < \dots < \lambda_k < \dots < \lambda_1 < +\infty$$

Lemma 6: For any $k \leq n$, equation $\mathbf{A}_k \boldsymbol{\theta}_k = \mathbf{0}$ has nonzero solutions $\boldsymbol{\theta}_k$ when $i = \lambda_k$. All the elements of $\boldsymbol{\theta}_k$ have the same sign.

Proof: We will prove Lemma 5 and Lemma 6 together using mathematical induction.

Base Case: When $k = 1$, we note that as indicated by Lemma 1, α_1 , the upper-left corner element of \mathbf{D} is positive. Moreover, the upper-left corner element of \mathbf{G}

$$g_1 = \sum_{0 \leq l \leq n} g_{1l}$$

is positive since \mathbf{G}_1 is positive definite, according to Lemma 4. Hence, $\det(\mathbf{A}_1) = 0$ has a positive root $\lambda_1 = g_1 / \alpha_1 < +\infty$. The corresponding nontrivial solution $\boldsymbol{\theta}_1$ can be any nonzero real number.

Induction Step: Suppose when $k = m - 1$, we have $\lambda_{m-1} < \dots < \lambda_2 < \lambda_1 < +\infty$. Besides, all the elements of $\boldsymbol{\theta}_{m-1}$ satisfying equation $\mathbf{A}_{m-1} \boldsymbol{\theta}_{m-1} = \mathbf{0}$ are non-zero and have the same sign. Without loss of generality, we assume these elements are all positive.

Induction for Lemma 5: let us first show that when $k = m$, we can construct a nonzero vector $\boldsymbol{\theta}$, such that

$$\boldsymbol{\theta}^T (\mathbf{G}_m - \lambda_{m-1} \mathbf{D}_m) \boldsymbol{\theta} < 0$$

We note that \mathbf{G}_m and \mathbf{D}_m can be represented as:

$$\mathbf{G}_m = \begin{pmatrix} \mathbf{G}_{m-1} & -\mathbf{g} \\ -\mathbf{g}^T & g_m \end{pmatrix}, \mathbf{D}_m = \begin{pmatrix} \mathbf{D}_{m-1} & \mathbf{0} \\ \mathbf{0}^T & \alpha_m \end{pmatrix}$$

Let us construct $\boldsymbol{\theta} = (\boldsymbol{\theta}_{m-1}^T, x)^T$ where x is a positive number.

We have

$$\begin{aligned} & \boldsymbol{\theta}^T (\mathbf{G}_m - \lambda_{m-1} \mathbf{D}_m) \boldsymbol{\theta} \\ &= (g_m - \lambda_{m-1} \alpha_m) \cdot x^2 - 2\mathbf{g}^T \boldsymbol{\theta}_{m-1} \cdot x + \boldsymbol{\theta}_{m-1}^T (\mathbf{G}_{m-1} - \lambda_{m-1} \mathbf{D}_{m-1}) \boldsymbol{\theta}_{m-1} \\ &= (g_m - \lambda_{m-1} \alpha_m) \cdot x^2 - 2\mathbf{g}^T \boldsymbol{\theta}_{m-1} \cdot x \end{aligned}$$

According to Lemma 4, matrix \mathbf{G}_m is an irreducible Stieltjes matrix. Hence, vector \mathbf{g} can only contain nonnegative element.

Furthermore, at least one element must be positive. Base on the induction of Lemma 6, all the elements of $\boldsymbol{\theta}_{m-1}$ are positive. As a result, $2\mathbf{g}^T \boldsymbol{\theta}_{m-1}$ must be a positive number. Hence, when x is small enough,

$$\boldsymbol{\theta}^T (\mathbf{G}_m - \lambda_{m-1} \mathbf{D}_m) \boldsymbol{\theta} < 0$$

The above inequality means matrix \mathbf{A}_m is not positive definite when $i = \lambda_{m-1}$. On the other hand, the induction hypothesis $\lambda_{m-1} < \dots < \lambda_2 < \lambda_1$ indicates that when $i = \lambda_{m-1}$, $\det(\mathbf{A}_k) \geq 0$ for any $1 \leq k \leq m - 1$. Hence, the fact that \mathbf{A}_m is not positive definite indicates $\det(\mathbf{A}_m) < 0$ when $i = \lambda_{m-1}$. On the other hand, we note that when $i = 0$, $\det(\mathbf{A}_m) = \det(\mathbf{G}_m) > 0$. Since $\det(\mathbf{A}_m)$ is a continuous real value function of i , equation $\det(\mathbf{A}_m) = 0$ must has a positive root $\lambda_m < \lambda_{m-1}$. This proves the induction hypothesis of Lemma 5 for $k = m$.

Induction for Lemma 6: Denote $\boldsymbol{\theta}_m = (\mathbf{v}_{m-1}^T, v_m)^T$, when $i = \lambda_m$, $\mathbf{A}_m \boldsymbol{\theta}_m = \mathbf{0}$ can be written as

$$\mathbf{A}_m \boldsymbol{\theta}_m = \begin{pmatrix} \mathbf{G}_{m-1} - \lambda_m \mathbf{D}_{m-1} & -\mathbf{g} \\ -\mathbf{g}^T & g_m - \lambda_m \alpha_m \end{pmatrix} \begin{pmatrix} \mathbf{v}_{m-1} \\ v_m \end{pmatrix} = \mathbf{0}$$

Hence, $\mathbf{A}_m \boldsymbol{\theta}_m = \mathbf{0}$ is equivalent to the following two equations:

$$\begin{aligned} & (\mathbf{G}_{m-1} - \lambda_m \mathbf{D}_{m-1}) \cdot \mathbf{v}_{m-1} = v_m \mathbf{g} \\ & \mathbf{g}^T \cdot \mathbf{v}_{m-1} = (g_m - \lambda_m \alpha_m) v_m \end{aligned}$$

If v_m is zero, $v_m \mathbf{g}$ must be a zero vector. On the other hand, in the induction step for Lemma 5, we have just proven that $\lambda_m < \lambda_{m-1}$, which means $\mathbf{G}_{m-1} - \lambda_m \mathbf{D}_{m-1}$ is positive definite. Hence, \mathbf{v}_{m-1} must be a zero vector. Therefore, in a nontrivial solution, $v_m \neq 0$. Without loss of generality, let us assume $v_m > 0$. Since \mathbf{G} is a fully irreducible Stieltjes matrix, vector $\mathbf{g} > \mathbf{0}$. As a result, vector $v_m \mathbf{g} > \mathbf{0}$. According to lemma 2, vector $\mathbf{v}_{m-1} \gg \mathbf{0}$. This proves the induction hypothesis of Lemma 6 for $k = m$.

Conclusion: Based on the above discussion, Lemma 5 and Lemma 6 hold true. ■

Lemma 7. The smallest positive root λ_n of equation $\det(\mathbf{A}) = 0$ is equal to the following infimum.

$$\lambda = \inf \left\{ \frac{\boldsymbol{\theta}^T \mathbf{G} \boldsymbol{\theta}}{\boldsymbol{\theta}^T \mathbf{D} \boldsymbol{\theta}} \mid \boldsymbol{\theta}^T \mathbf{D} \boldsymbol{\theta} > 0 \right\} \quad (\text{A2})$$

Proof: Firstly, let us show that $\lambda \leq \lambda_n$. Since λ_n is the smallest positive root of $\det(\mathbf{A}) = 0$, there exists $\boldsymbol{\theta}_n \neq \mathbf{0}$ such that $\mathbf{A} \boldsymbol{\theta}_n = (\mathbf{G} - \lambda_n \mathbf{D}) \boldsymbol{\theta}_n = \mathbf{0}$. Hence, $\lambda_n = \boldsymbol{\theta}_n^T \mathbf{G} \boldsymbol{\theta}_n / \boldsymbol{\theta}_n^T \mathbf{D} \boldsymbol{\theta}_n$. Moreover, according to Lemma 5, λ_n is a positive number. $\boldsymbol{\theta}_n^T \mathbf{G} \boldsymbol{\theta}_n$ is a positive number also since \mathbf{G} is positive definite. Hence, $\boldsymbol{\theta}_n^T \mathbf{D} \boldsymbol{\theta}_n > 0$. Therefore, $\lambda_n = \boldsymbol{\theta}_n^T \mathbf{G} \boldsymbol{\theta}_n / \boldsymbol{\theta}_n^T \mathbf{D} \boldsymbol{\theta}_n \geq \lambda$.

Secondly, we show that $\lambda \geq \lambda_n$. If this is not the case, according to Lemma 5, for any $k = 1, 2, \dots, n$, $\det(\mathbf{G}_k - \lambda \mathbf{D}_k) > 0$. Hence, $\mathbf{G} - \lambda \mathbf{D}$ is positive definite. Then, for any nonzero vector $\boldsymbol{\theta}$, $\boldsymbol{\theta}^T (\mathbf{G} - \lambda \mathbf{D}) \boldsymbol{\theta} > 0$, i.e., $\boldsymbol{\theta}^T \mathbf{G} \boldsymbol{\theta} / \boldsymbol{\theta}^T \mathbf{D} \boldsymbol{\theta} > \lambda$. However, this contradicts with the definition of λ .

Based on the above discussion, λ_n and λ are identical. ■

Since λ_n and λ are identical, we will use them interchangeably in the rest of the proofs.

Theorem 2: Given λ as defined in Lemma 7, matrix \mathbf{A} has the following properties:

- 1) For any $i \in [0, \lambda)$, \mathbf{A} is positive definite.
- 2) When $i = \lambda$, \mathbf{A} is singular and semidefinite.
- 3) For any $i \in [\lambda, +\infty)$, \mathbf{A} is not positive definite.

Proof. 1) Since λ is the smallest positive root of $\det(\mathbf{A}) = 0$, it is obvious that for any $i \in [0, \lambda)$, \mathbf{A} is positive definite.

2) When $i = \lambda$, \mathbf{A} is singular since $\det(\mathbf{A}) = 0$. In the meanwhile, Lemma 4 and Lemma 6 indicate $\lambda_1 > \lambda_2 > \dots > \lambda_k > \dots > \lambda_n = \lambda$. Thus, for any $k < n$, $\det(\mathbf{A}_k) > 0$ when $i = \lambda$. Hence, \mathbf{A} is semidefinite when $i = \lambda$.

3) When $i > \lambda$, according to the definition of λ given in Lemma 7, there is a nonzero $\boldsymbol{\theta}$ satisfying $\boldsymbol{\theta}^T \mathbf{G} \boldsymbol{\theta} / \boldsymbol{\theta}^T \mathbf{D} \boldsymbol{\theta} = \lambda < i$. That is, $\boldsymbol{\theta}^T (\mathbf{G} - i\mathbf{D}) \boldsymbol{\theta} < 0$. Hence, for any $i \in [\lambda, +\infty)$, \mathbf{A} is not positive definite. ■

Before proving Theorem 3, we first prove that following lemmas:

Lemma 8: When $i = \lambda$, if $\mathbf{A}\boldsymbol{\theta} \neq \mathbf{0}$, then $\boldsymbol{\theta}^T \mathbf{A}\boldsymbol{\theta} > 0$.

Proof. According to Lemma 5 and Lemma 7, $\det(\mathbf{A}) = 0$ when $i = \lambda$. Moreover, we note that \mathbf{A} is a symmetric matrix. Hence, there exists an orthogonal matrix \mathbf{P} , such that \mathbf{A} can be eigendecomposed to be

$$\mathbf{A} = \mathbf{P}^T \mathbf{Q} \mathbf{P} = \mathbf{P}^T \begin{pmatrix} \mu_1 & & & 0 \\ & \mu_2 & & 0 \\ & & \mu_k & \\ & & & \mu_{n-1} \\ 0 & & & & 0 \end{pmatrix} \mathbf{P}$$

where $\mu_k > 0$ for $k = 1, 2, \dots, n-1$. Given any $\boldsymbol{\theta} \in \mathbf{R}^n$, denote $\mathbf{y} = \mathbf{P}\boldsymbol{\theta}$,

$$\boldsymbol{\theta}^T \mathbf{A} \boldsymbol{\theta} = (\mathbf{P}\boldsymbol{\theta})^T \mathbf{Q} (\mathbf{P}\boldsymbol{\theta}) = \mathbf{y}^T \mathbf{Q} \mathbf{y} = \sum_{k=1}^{n-1} \mu_k y_k^2.$$

Hence, $\boldsymbol{\theta}^T \mathbf{A} \boldsymbol{\theta} = 0$ if and only if $\mathbf{y} = y_n \cdot \mathbf{u}_n$. Here $\mathbf{u}_n = (0, \dots, 0, 1)^T$ and y_n can be any real value. Therefore, $\boldsymbol{\theta} = \mathbf{P}^{-1} \mathbf{y} = y_n \mathbf{P}^{-1} \mathbf{u}_n$. For this $\boldsymbol{\theta}$ vector, we have $\mathbf{A}\boldsymbol{\theta} = \mathbf{A} \cdot y_n \mathbf{P}^{-1} \mathbf{u}_n = y_n (\mathbf{P}^T \mathbf{Q} \mathbf{P}) \mathbf{P}^{-1} \mathbf{u}_n = y_n \mathbf{P}^T (\mathbf{Q} \mathbf{u}_n)$. It is easy to verify that $\mathbf{Q} \mathbf{u}_n = \mathbf{0}$. As a result, $\mathbf{A}\boldsymbol{\theta} = \mathbf{0}$. Note that \mathbf{A} is semidefinite. Therefore, for any given $\boldsymbol{\theta}$, if $\mathbf{A}\boldsymbol{\theta} \neq \mathbf{0}$, then $\boldsymbol{\theta}^T \mathbf{A} \boldsymbol{\theta} > 0$. ■

Lemma 9: Define \mathbf{U}_k to be a matrix where the element at the k^{th} row and k^{th} column is one while other elements being zeros. Matrix $\mathbf{B} = \mathbf{A} + \mathbf{U}_k$ is positive definite when $i = \lambda$.

Proof. For given any $\boldsymbol{\theta} \in \mathbf{R}^n$, we have

$$\boldsymbol{\theta}^T \mathbf{B} \boldsymbol{\theta} = \boldsymbol{\theta}^T (\mathbf{A} + \mathbf{U}_k) \boldsymbol{\theta} = \boldsymbol{\theta}^T \mathbf{A} \boldsymbol{\theta} + \boldsymbol{\theta}^T \mathbf{U}_k \boldsymbol{\theta}$$

If the k^{th} element of $\boldsymbol{\theta}$ is zero, according to Lemma 6, when $i = \lambda$, $\mathbf{A}\boldsymbol{\theta} \neq \mathbf{0}$. According to Lemma 8, we have $\boldsymbol{\theta}^T \mathbf{A} \boldsymbol{\theta} > 0$. On the other hand, $\boldsymbol{\theta}^T \mathbf{U}_k \boldsymbol{\theta} = 0$. Hence, $\boldsymbol{\theta}^T \mathbf{B} \boldsymbol{\theta} > 0$.

If the k^{th} element of $\boldsymbol{\theta}$ is not zero, we have $\boldsymbol{\theta}^T \mathbf{A} \boldsymbol{\theta} \geq 0$ since \mathbf{A} is semidefinite according to Theorem 2. Moreover, $\boldsymbol{\theta}^T \mathbf{U}_k \boldsymbol{\theta} > 0$. Hence we still have $\boldsymbol{\theta}^T \mathbf{B} \boldsymbol{\theta} > 0$.

Therefore, matrix \mathbf{B} is positive definite. ■

Lemma 10: When $i = \lambda$, $\det(\mathbf{A}_{kl}) > 0$ for any $1 \leq k, l \leq n$.

Proof: Define $\mathbf{B} = \mathbf{A} + \mathbf{U}_k$ as in Lemma 9. Denote the matrix form by removing from \mathbf{B} its k^{th} row and l^{th} column by \mathbf{B}_{kl} , \mathbf{A}_{kl} and \mathbf{B}_{kl} must be identical. On the other hand, according to Lemma 9, \mathbf{B} is positive definite when $i = \lambda$. Further, it is easy to verify that \mathbf{B} is a fully irreducible Stieltjes matrix. According to Lemma 3, every element of $\mathbf{C} = \mathbf{B}^{-1}$ is positive. Using Cramer's rule, we have $\det(\mathbf{B}_{kl}) = c_{kl} \det(\mathbf{B}) > 0$, where

c_{kl} is the element at the k^{th} row and l^{th} column of \mathbf{C} . This leads to $\det(\mathbf{A}_{kl}) > 0$. ■

Theorem 3: Denote the element of \mathbf{H} in the k^{th} row and the l^{th} column (as a function of i) as $h_{kl}(i)$. For any $1 \leq k, l \leq n$, we have

$$\lim_{i \rightarrow \lambda^-} h_{kl}(i) = +\infty$$

Proof: Applying Cramer's rule, we have

$$\lim_{i \rightarrow \lambda^-} h_{kl}(i) = \lim_{i \rightarrow \lambda^-} \frac{\det(\mathbf{A}_{kl})}{\det(\mathbf{A})}$$

According to Lemma 10 and Theorem 2, when $i = \lambda$,

$$\lim_{i \rightarrow \lambda^-} \det(\mathbf{A}_{kl}) > 0, \quad \lim_{i \rightarrow \lambda^-} \det(\mathbf{A}) = 0$$

Therefore,

$$\lim_{i \rightarrow \lambda^-} h_{kl}(i) = +\infty. \quad \blacksquare$$

Conjecture 1: Given an $n \times n$ positive definite Stieltjes matrix \mathbf{S} , denote $\mathbf{R} = \mathbf{S}^{-1}$. Denoting the k^{th} and l^{th} row vector of \mathbf{R} by \mathbf{r}_k and \mathbf{r}_l , then $\text{DIAG}(\mathbf{r}_k) \cdot \mathbf{R} \cdot \text{DIAG}(\mathbf{r}_l)$ is positive definite for any $1 \leq k, l \leq n$.

Theorem 4: If Conjecture 1 holds true, then for every $1 \leq k, l \leq n$, $h_{kl}(i)$ of matrix \mathbf{H} is a convex function of i over $[0, \lambda)$.

Proof: According to matrix analysis theory, we have

$$\begin{aligned} \mathbf{H}'(i) &= \frac{d^2 \mathbf{H}}{di^2} = \frac{d}{di} \frac{d\mathbf{H}}{di} = \frac{d}{di} \left(\mathbf{H} \frac{d\mathbf{H}^{-1}}{di} \mathbf{H} \right) = \frac{d}{di} (\mathbf{H} \mathbf{D} \mathbf{H}) \\ &= \mathbf{H} \mathbf{D} \frac{d\mathbf{H}}{di} + \frac{d\mathbf{H}}{di} \mathbf{D} \mathbf{H} = 2\mathbf{H} \mathbf{D} \mathbf{H}' \mathbf{D} \mathbf{H} \end{aligned}$$

Denote the k^{th} and l^{th} row vector of \mathbf{H} by \mathbf{h}_k and \mathbf{h}_l , the element in the k^{th} row and l^{th} column of \mathbf{H} as a function of i by $h_{kl}(i)$, the vector formed by the elements in the main diagonal of \mathbf{D} by \mathbf{d} , we have

$$\begin{aligned} h_{kl}'(i) &= 2\mathbf{h}_k^T \cdot \mathbf{D} \mathbf{H} \mathbf{D} \cdot \mathbf{h}_l = 2\mathbf{h}_k^T \cdot \text{DIAG}(\mathbf{d}) \cdot \mathbf{H} \cdot \text{DIAG}(\mathbf{d}) \cdot \mathbf{h}_l \\ &= 2\mathbf{d}^T (\text{DIAG}(\mathbf{h}_k^T) \cdot \mathbf{H} \cdot \text{DIAG}(\mathbf{h}_l)) \mathbf{d} \end{aligned}$$

According to Theorem 2, for any $i \in [0, \lambda)$, \mathbf{A} is a positive definite Stieltjes matrix. Then, $(\text{DIAG}(\mathbf{h}_k) \cdot \mathbf{H} \cdot \text{DIAG}(\mathbf{h}_l))$ is positive definite if Conjecture 1 holds. As a result, $h_{kl}(i)$ is positive over $[0, \lambda)$, which means $h_{kl}(i)$ is a convex function of i over $[0, \lambda)$. ■

Remark: At the end, we remarks that the theoretical analysis presented in Appendix A can be viewed as an extension of the classical eigenvalue/eigenvector theory in linear algebra. A general diagonal matrix \mathbf{D} replaces the role of the identity matrix in the classical eigenvalue/eigenvector theory. The value λ is similar to the concept of the smallest eigenvalue. The definition of λ given in Expression (A2) generalizes the concept of Rayleigh's quotient.

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