A 65nm Implantable Gesture Classification SoC for Rehabilitation with Enhanced Data Compression and Encoding for Robust Neural Network Operation Under Wireless Power Condition

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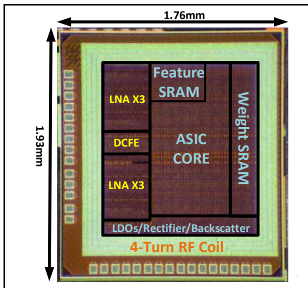
Two million amputee patients in the US rely on prosthetic devices for assistance or rehabilitation. Compared with skin-mounted devices, muscle implantable devices offer better signal quality, lower noise inference, less wires and skin irritation. In prior works, a near-infrared powered neural recoding system was demonstrated with optical light TX/RX [1]. An Ultrasound powered neural recorder with AM backscatter was presented [2]. Stimulus systems powered by on/off-chip RF coil via inductive link were also developed [3-5]. However, prior implantable systems only perform neural recording with neural signals transferred to external devices for further classification. As in Fig. 1, the transmission of raw neural signals consumes high power and suffers from high bit errors. In addition, external devices may not meet the millisecond classification latency needed for real-time prosthetic control. Hence, a fully integrated solution with embedded classifiers for EMG-based gesture classification offers significant benefits of reduced transmission efforts, low latency, and low error rate. However, a neural network (NN) classifier under wireless power poses challenges of robustly sending weights into the device under noisy conditions. This work, for the first time, presents a fully integrated implantable wireless powered SoC with an embedded NN classifier. The contributions of this work include (1) a wireless powered SoC with NN classifiers and on-chip coil is presented paving the way to embed AI techniques into implantable devices; (2) To reduce the NN weight for sending into the chip at startup, Huffman coding and low-rank singular value decomposition (SVD) techniques are implemented reducing data volume by 29%; (3) New activity detection for NN computing and adaptive power control under unstable wireless power are developed improving power efficiency of the system by 45%; (4) A unique data encoding strategy is also utilized to reduce the bit error rate by orders of magnitudes.

Fig. 2 shows the chip architecture. A 4-turn on-chip coil on the RDL layer receives wireless power via an inductive link at 125 MHz. The input data signals, e.g. instructions or neural network weights are ASK modulated into the RF power signal. A CMOS full bridge rectifier works with a 100 nF SMD capacitor to establish a resonance for generating rectified DC voltage. Three LDOs run under 2.5V to generate 0.75 V, 1 V, and 1.8 V for on-chip digital ASICs, analog circuits, and IO circuits, respectively. High PSRR reference generators are used for references of analog modules. 6-channel differential LNAs with variable gain from 24 dB to 54 dB are used for the EMG amplification. 48 time-domain features are extracted for use by NN classification and also stored in a feature SRAM bank for data logging and off-chip training. Five special techniques are developed in the "AI-compute" core for embedded classification, including (1) Huffman coding, and (2) SVD, both for weight reduction, (3) special coding for low error rate UART receiver, (4) adaptive control under wireless power, (5) new activity detection for bypassing classifier. All input features propagate through a 3-layer fully connected neural network to generate final gesture labels transmitted using LED light for communication, similar to [1]. The use of LED light brings benefits of low power and tolerance of interference under wireless power compared with backscattering techniques.

Fig. 3 shows the signal processing flow of the chip. After analog amplification and data conversion, 48 8-bit time-domain features are extracted, including mean, variance, slope sign changes, zero crossing, and 4 level histograms per channel. After each sampling window of 100ms, the input features are passed through a three-layer neural network with 48/32/16 neurons at each layer to generate the output label of users' gesture intention for control of the prosthesis within targeted 5ms. Two special low power techniques are implemented shown in Fig. 3. A "new activity detection" circuit (NAD) is used for "event" based operation. As patients spend most time idle or in a static position, a power-hungry neural network can be suspended if very similar features are detected by checking 24 histogram features with the cached feature from the last sampling window. If the difference is below a preset threshold, the previous label is sent out without new classification, leading to 45% overall power saving. Adaptive power control is also used to adjust the chip power under wireless conditions. A power detector measures the output voltage from the rectifier and guides the analog circuits into one of the four power modes from 58% to 100% of power by adjusting LNAs and LDOs setting at a trade-off between power and LNA's performance.



Die micrograph.

To cope with the challenges of wirelessly download of NN weights to the chip, advanced data compression techniques are implemented as in Fig. 4. An SVD scheme is used to decompose a high dimensional matrix into a low dimensional matrix for data transmission. The received matrix is recovered on the chip through a matrix reconstruction unit. Huffman coding is also adopted to reduce total weight transmission. More frequent data patterns are coded with shorter representations stored in a Lookup Table (LUT). The final weights are recovered from a Huffman decoder on the chip. As shown in Fig.4, a 30% reduction in data transmission is achieved by using these compression schemes. To control the wireless chip, specially coded instruction commands are used. The 18-bit instruction code reduces the chance of wrong instruction being triggered by four orders of magnitude from the simulation. A special UART protocol was also used to improve the noise resiliency by resetting the receiving sequence after every falling edge. Hence, the tolerance of mismatch on clock frequency between transmitter and receiver is improved from ~0.5% to 40%, significantly reducing error probability. The drop in data rate has a negligible impact because no high-volume data transmission is needed at normal operation. The implemented chip can classify gestures from pre-recorded EMG signals with 82% overall accuracy with five gestures.

Figure 5 shows the measurement results from a 65nm test chip. 25 kHz ASK modulated data signals with 125MHz wireless power were sent from the external antenna to the on-chip coil via inductive link. A 500-mV power envelope signal was forming at the output of the rectifier. The power envelope detector generates the corresponding signal triggering the digital UART module to latch the data. The output labels are generated each 100ms window and detected by the external photodetector as shown in the measured waveforms, which also include measured amplified EMG signal. The chip power breakdown shows that the digital core consumes most of the power at 135 uW (with a peak power of 330uW), and the rest of IO/LDO and LNAs consume 10 and 18 uW, respectively. The wireless measurement setup is also shown in Fig.5. Fig. 6 compares this work with prior wireless chips or biomedical chips with an integrated classifier. This work is the first work that fully integrates analog front-end, digital classifier, and wireless power with an on-chip coil. To address issues of "AI-Compute" in the implantable device under wireless conditions, the applied data compression and coding techniques effectively reduced data transmission by 30%, decreased power by 45% through activity detection, and reduced analog power by 42% by adaptive power control under wireless conditions.

Acknowledgements:
This work was supported in part by NSF grant CNS-1816870.

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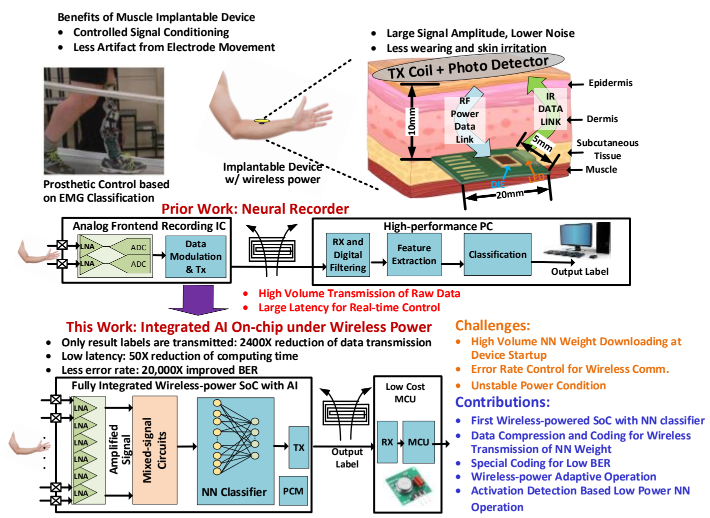

Fig. 1. Wireless EMG gesture classification system overview (top); Conventional gesture classification flow versus the fully integrated gesture classification flow in this work (bottom).

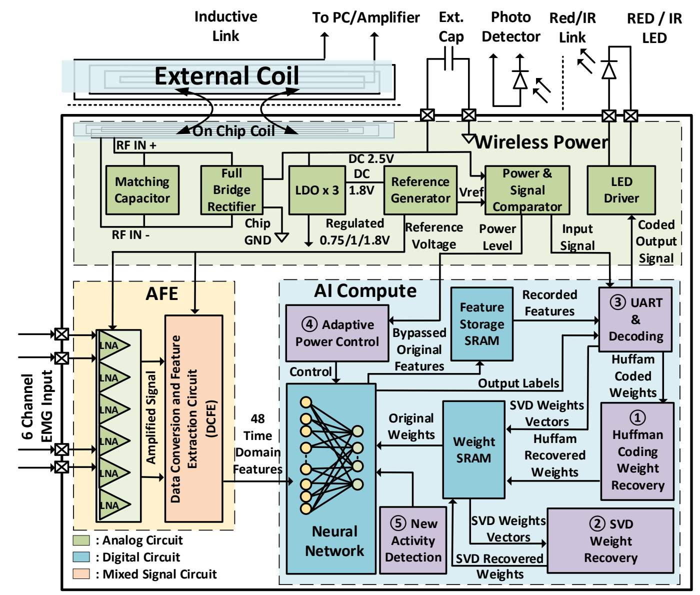

Fig. 2. Block diagram of the wireless gesture classification SoC.

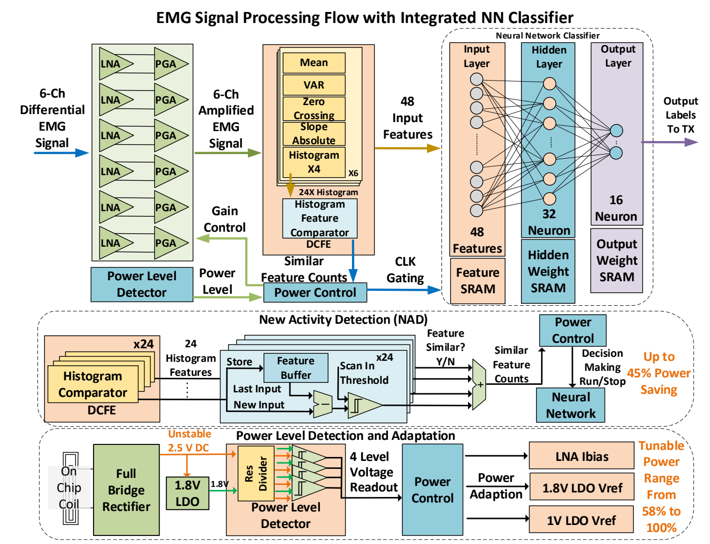

Fig. 3. Neural network architecture and signal processing flow (top). New activity detection (NAD) flow (middle). Power level detection and adaptation flow (bottom).

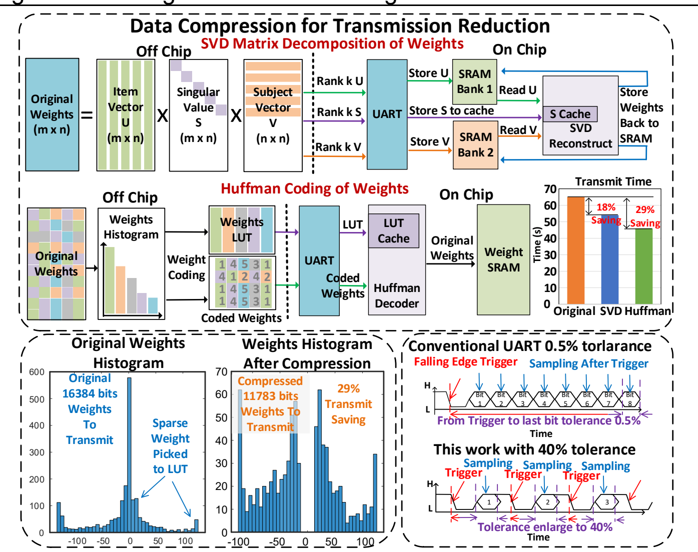

Fig. 4. SVD (de)compression flow (top). Huffman coding (de)compression flow and transmit time saving (middle, bottom left). Special UART scheme for freq. mismatch (bottom right).

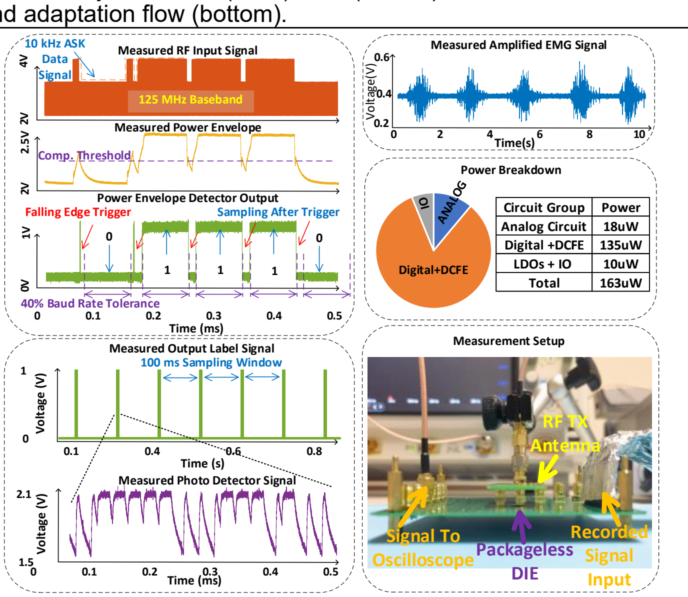

Fig. 5. Measurement results with signal waveforms and power breakdown.

	ISSCC'20[1]	ISSCC'19[2]	ISSCC'18[3]	ISSCC'19[4]	ISSCC'21[5]	ISSCC'21[6]	This Work
Technology (nm)	180	65	350	180	130	65	65
Area(mm²)	0.0323	0.225	1	13.67	7.02	1.74	3.4
Supply Voltage	1.5	1	1.8	12./1.8/3.3	0.5-1.6	0.75	0.7/1/1.8
CLK Frequency						500KHz	10MHz
Total Power(uW)	0.74	28.8	2.8	0.83mW	810	30	163
Powering Method	Optical	Ultrasound	Inductive Link	Inductive Link	Inductive Link	DC	Inductive Link
Wireless Power	YES	YES	YES	YES	YES	N/A	YES
Wireless Data	YES	YES	YES	YES	YES	N/A	YES
On Chip Coil	NO	NO	NO	NO	YES	N/A	YES
Data TX method	Optical	AM Backscatter	Off Chip Coil	Off Chip Coil	On Chip Coil	N/A	Optical
Task	Neural Recording	Neural recording	Optical Stimuation	Epilepsy detection	Peripheral Nerve Recording	EEG / Seizure Detection / EMG	Gesture Classification
Classifier	N/A	N/A	N/A	Linear Least Squares	N/A	Neural Network	Neural Network
No. of Analog Channel	1	1		2	64		6
Analog Power/ Channel (uW)	0.51	4	N/A	15.5	0.14	N/A	3
Area/Channel(mm²)					0.01		0.07
Bandwidth(Hz)	180-950	5000		100	5.5k		4k
Gain(dB)	69	24		27			24-54

Fig. 6. Comparison table with prior works.