CHUAN LIN

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INTEREST

Timing optimization, Algorithms, Formal verification, Physical design.

EDUCATION

Ph.D. Northwestern University - June 2006 (Expected)

Major:	Computer Engineering
Proposal:	Timing Optimization Algorithms for Sequential Circuits
Advisor:	Professor Hai Zhou
GPA overall:	3.98/4.0

B.S. Tsinghua University, Beijing, China - June 2002

Major:	Microelectronics
GPA overall:	88.1/100
GPA in major:	91.0/100

HONORS AND AWARDS

- Murphy Fellowship - Northwestern University, 2002
- Outstanding Graduate Award - Tsinghua University, 2002
- Tsinghua 2nd Prize Scholarship - Tsinghua University, 2001
- Tsinghua 1st Prize Scholarship - Tsinghua University, 2000
- Top 50 - National Physics Olympiad, China, 1998

WORKING EXPERIENCE

Sept 2002-Present: Research Assistant, Computer Engineering, Northwestern University.

- Developed optimal wire retiming algorithms for clock period minimization;
- Proposed an efficient representation for clock schedule verification and a framework to control crosstalk via latch/flop trade-off;
- Developed a clustering algorithm for processing rate optimization;
- Research on clock scheduling and skew optimization;
- Research on floorplan and placement using network flow techniques.

Summer 2005: Intern, System Level Synthesis Group, Calypto Design Systems Inc, Santa Clara, CA.

- Developed and implemented an optimal delay budgeting algorithm for sequential circuits based on convex cost integer dual network flow formulation.

Fall 2005, Winter 2005, Fall 2004, Fall 2003, Fall 2002: Teaching Assistant for various ECE courses.

Sept 2001-June 2002: Research Assistant, Institute of Microelectronics, Tsinghua University.

- Developed a low-power quadrature converter and CMOS mixer for 70MHZ-600MHZ wireless network RF chip set based on HFA3783 norms.

PUBLICATIONS

Journal articles

1. Hai Zhou and **Chuan Lin**, Retiming for Wire Pipelining in System-On-Chip. *IEEE Transactions on Computer-Aided Design (TCAD)*, 23(9), pp. 1338-1345, September 2004.
2. **Chuan Lin** and Hai Zhou. Wire Retiming as Fixpoint Computation. *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*. 13(12), December 2005.
3. **Chuan Lin** and Hai Zhou. Optimal Wire Retiming Without Binary Search. *IEEE Transactions on Computer-Aided Design (TCAD)*. Accepted for publication.
4. **Chuan Lin** and Hai Zhou. Trade-off between Latch and Flop for Min-Period Sequential Circuit Designs with Crosstalk. Under revision for *IEEE Transactions on Computer-Aided Design (TCAD)*.
5. **Chuan Lin**, Jia Wang, and Hai Zhou. Clustering for Processing Rate Optimization. Submitted to *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*.

Conference papers

6. **Chuan Lin** and Hai Zhou. Retiming for Wire Pipelining in System-On-Chip. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD'03)*, San Jose, CA, 2003.
   (Best paper award nominee)
7. **Chuan Lin** and Hai Zhou. Wire Retiming for System-On-Chip by Fixpoint Computation. *Design Automation and Test in Europe (DATE'04)*, Paris, France, 2004.
8. **Chuan Lin** and Hai Zhou. Optimal Wire Retiming Without Binary Search. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD'04)*, San Jose, CA, 2004.
9. **Chuan Lin** and Hai Zhou. Trade-off between Latch and Flop for Min-Period Sequential Circuit Designs with Crosstalk. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD'05)*, San Jose, CA, 2005.
10. **Chuan Lin**, Jia Wang, and Hai Zhou. Clustering for Processing Rate Optimization. *IEEE/ACM International Conference on Computer-Aided Design (ICCAD'05)*, San Jose, CA, 2005.
11. **Chuan Lin** and Hai Zhou. An Efficient Retiming Algorithm Under Setup and Hold Constraints. *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU'06)*, San Jose, CA, 2006.
12. **Chuan Lin**, Hai Zhou, and Aiguo Xie. Design Closure Driven Delay Relaxation Based on Convex Cost Network Flow. *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU'06)*, San Jose, CA, 2006.
13. **Chuan Lin** and Hai Zhou. Clock Skew Scheduling with Delay Padding for Prescribed Skew Domains. Submitted to *ACM Great Lakes Symposium on VLSI*.

Technical reports

14. **Chuan Lin** and Hai Zhou. Trade-off between Latch and Flop for Min-Period Sequential Circuit Designs with Crosstalk. EECS Department, Northwestern University, TR-NUCAD-2005-01, 2005.
15. **Chuan Lin**, Jia Wang, and Hai Zhou. Clustering for Processing Rate Optimization. EECS Department, Northwestern University, TR-NUCAD-2005-02, 2005.

PROFESSIONAL SERVICE

- Reviewer for IEEE Transactions on Computer-Aided Design (TCAD), Design Automation Conference (DAC), International Conference on Computer-Aided Design (ICCAD), International conference on Computer Design (ICCD), Asia and South Pacific Design Automation Conference (ASP-DAC), and International Symposium on Physical Design (ISPD).

RELEVANT COURSES

- Design and Analysis of Algorithms, Design Automation in VLSI CAD, Advanced VLSI Algorithms
- Design and Analysis of VLSI circuits, VLSI Systems Design, VLSI High Performance Issues
- Advanced Computer Architecture, Multiprocessor Design, ASIC and FPGA Design
- Mathematical Programming, Mathematical Logic, Nonlinear Programming, Integer Programming
- Formal Techniques in Design and Verification of Digital Systems, System Specification in TLA+
- Compiler Construction, Computer Hardware, Layout Design/Extraction, Semiconductor Physics

COMPUTER SKILLS

- Languages - C/C++, VHDL/Verilog, Perl, Unix Shell Scripts, Tcl
- Softwares - emacs, gdb, gcc, Makefile
- Tools - Synopsys, Cadence, Mentor Graphics, HSPICE
- Architectures - Intel 80x86, MIPS

REFERENCES

Professor Hai Zhou
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