INSTRUCTION-LEVEL TIMING ERROR PREDICTION MODELLING



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ABSTRACT

In this project, we build an instruction-level timing error prediction model for a 5-stage pipelined ALPHA processor which supports timing speculation. This model predicts that an instruction has timing error given the information of instruction sequence and data usage.

INTRODUCTION

Timing error is defined as a violation in circuit-level timing constraints during program execution. In traditional processors, timing error may cause catostrophic system failure. Processors which support timing speculation are augmented with timing-error detection and correction techniques so that they able to recover from timing errors.

However, the recovery cost is very high. Also, based on some existing work, for a specific processor, timing error is a strong function of programs. Therefore, an effective timing-error prediction model can be built based on the information of how the programs are executed on the processor. Then, the compiler can apply this model to generate codes that have lower probability of producing timing errors by using instruction scheduling and instruction selection. Moreover, if the model is implemented in the hardware, it can predict timing error at run-time. With some padding techniques, it can avoid the full recovery cost due to timing errors.

In this project, we use machine learning algorithms to build an instruction-level timing error prediction model for a 5-stage pipelined AL-PHA processor which supports timing speculation. This model predicts that an instruction has timing error given the information of instruction sequence and data usage.

REFERENCES

[1] J. Xin and R. Joseph. Identifying and predicting timingcritical instructions to boost timing speculation. In MICRO-44 '11, pages 128–139, New York, NY, USA, 2011. ACM.

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LEARNING PROCESS

• Dataset

We use ten instruction-level test programs to build ten test sets. In each set, we pick nine programs for trainning and the other one for testing.

ST PROGRAM #3: compute first 16 fibonacci numb

NO.	Name	Description
1	сору	copy memory contents of N elements
2	objsort	object sorting algorithm
3	parsort	parsort algorithm
4	fib	compute nth fibonacci numbers
5	fib_rec	compute nth fibonacci number recursively
6	evens	compute even numbers that are less than n
7	insertion	insertion sorting
8	parallel	compute first n multiples of m
9	sort	bubble sorting
10	saxpy	integer SAXPY

Each instance in the training and testing sets consists of several parts, including the current instruction and (N-1) preceding instructions. N is defined as the instruction window size which means the number of instruction affect that if the current instruction produces a timing error. For operand data used in each instruction, we use both number and bits representation.

• Learning Algorithms

- * J48 Decision Tree
- * Multilayer Perceptron

• Sofware Packages

- * Synopsys tools
- * WEKA software packages

CONCLUSIONS & FUTURE DIRECTION

Both J48 Decision Tree and Multilayer Perceptron algorithm are good to use to build models to predict timing errors. Each algorithm has its own advantages and disadvanges.

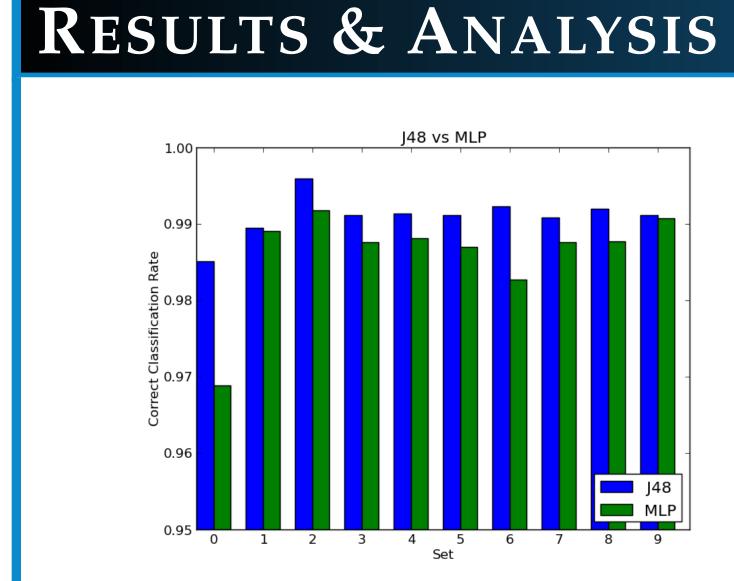
• J48 Decision Tree is slightly better. Building a model using Multilayer Perceptron takes much longer. • Instruction Window Size of 2 overperforms others.

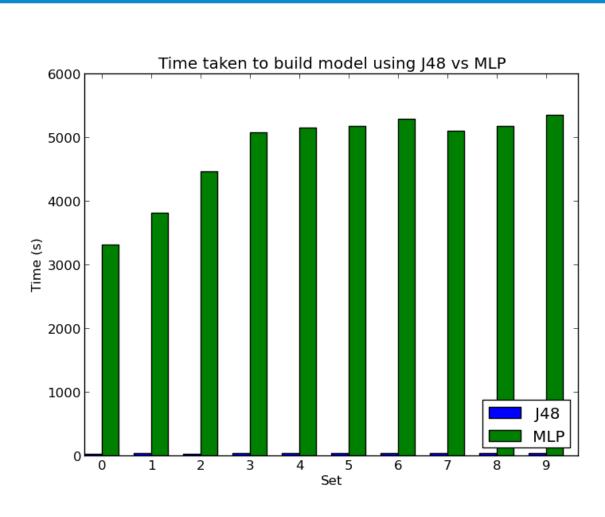
• The left figure shows the results of using 10-fold cross validation on the training set and validating using the testing set.

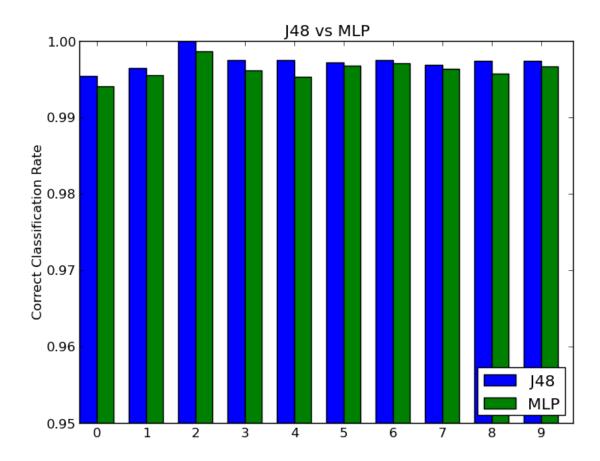
• Multilayer perceptron algorithm has less overfitting problem in our case.

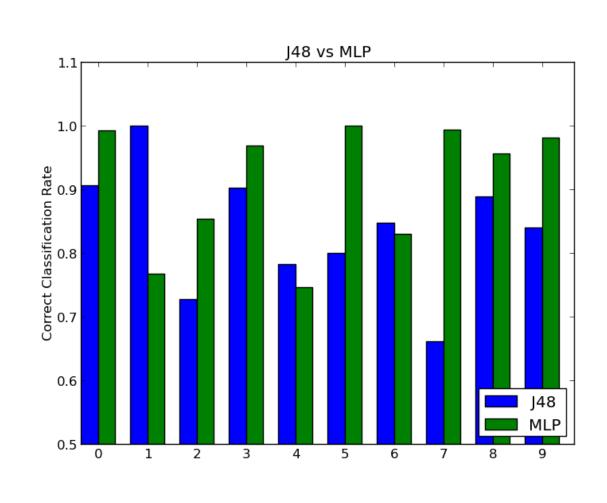
• The left figure has 10% error rate in the test program, while the right one has 20%. • This proves that when the rates change from 10% to 20%, a large portion of errors are caused by the values used in the program.

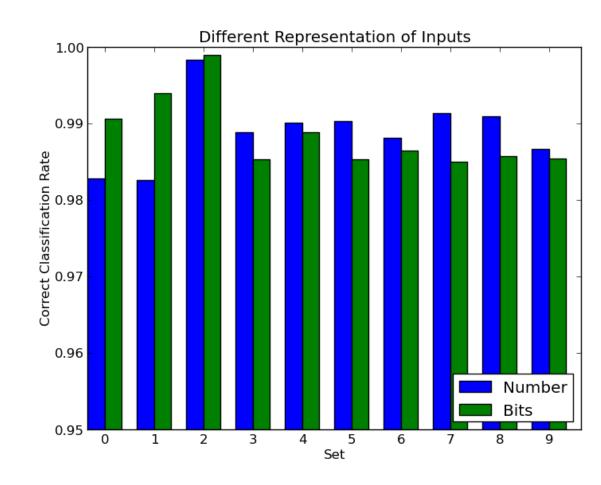
This timing error prediction model can be used either to improve the overall performance of a program or to study interesting characteristics of timing errors.

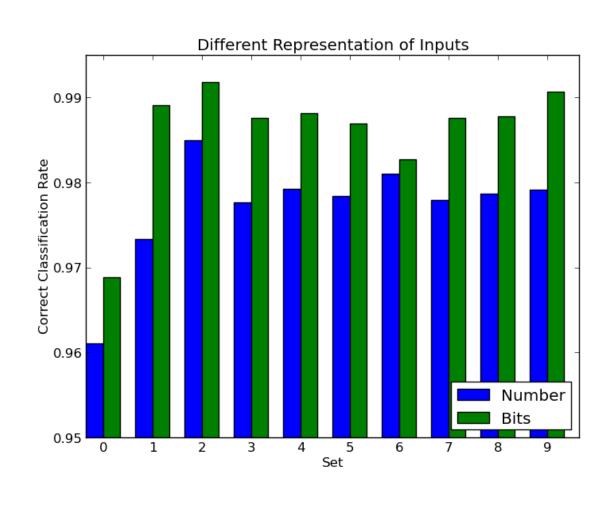




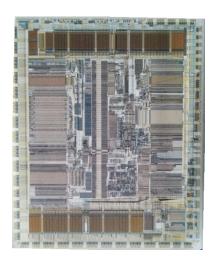


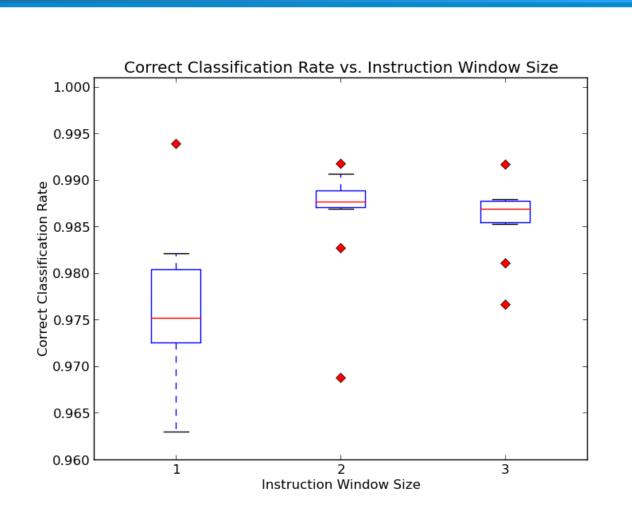






WEBSITE





All resources are available at http://users.eecs.northwestern.edu/ ~yfw492/eecs349/