

## EDUCATION

### University of California – Los Angeles

Ph.D., Computer Science Department

*August 2003*

### Northwestern University

M.S., Electrical and Computer Engineering Department

*May 2000*

### Bogazici University, Istanbul, Turkey

B.S., Department of Electrical and Electronic Engineering

*July 1998*

## EMPLOYMENT

### Northwestern University

Associate Professor, Dept. of Electrical Engineering and Computer Science  
Assistant Professor, Dept. of Electrical Engineering and Computer Science

*September 2009 - Present*  
*September 2003-September 2009*

### Fujitsu Laboratories of America, Inc., Sunnyvale, CA

Research Intern

*June - August 2001*

### University of California – Los Angeles

Research Assistant

*December 2000 – August 2003*

### Northwestern University

Research Assistant

*September 1998-December 2000*

## AWARDS AND HONORS

1. Distinguished Visitor, School of Computer Science, Complutense Universidad de Madrid, March-May 2010.
2. Best Paper Award Finalist, IEEE/ACM International Conference on Computer Aided Design (ICCAD) 2007
3. National Science Foundation CAREER Award (2006)
4. Searle Center for Teaching Excellence Junior Fellow (2006-2007)
5. Co-author of the Best Paper Award Nominee, IEEE/ACM Design Automation Conference (DAC) 2005
6. Co-author of the Best Paper Award Nominee, IEEE/ACM Design Automation Conference (DAC) 2001

## PUBLICATIONS

### Refereed Journal Publications

1. A. Varrenti, C. Zhou, A. Klock, S. Chyung, J. Long, S. Ogrenci Memik, M. Grayson, "Thermal Sensing with Lithographically Patterned Bimetallic Thin-Film Thermocouples", IEEE Electron Device Letters, Vol. 32, No. 6, pp. 818-820, 2011.
2. A. A. Del Barrio Garcia, S. Ogrenci Memik, M. C. Molina, J. M. Mendias, R. Hermida, "A Distributed Controller for Managing Speculative Functional Units in High Level Synthesis", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), Vol. 30, No. 3, pp. 350-363, 2011
3. J. Long, J.-C. Ku, S. Ogrenci Memik, Y. Ismail, "SACTA: A Self-Adjusting Clock Tree Architecture for Adapting to Thermal-Induced Delay Variation", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 18, No. 9, pp. 1323-1336, 2010.
4. S. Liu, S. Ogrenci Memik, Y. Zhang, G. Memik, "An Approach for Adaptive DRAM Temperature and Power Management", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 18, No. 4, pp. 684-688, April 2010.
5. M. Ni, S. Ogrenci Memik, "A Fast Heuristic Algorithm for Multi-Domain Clock Skew Scheduling", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 18, No. 4, pp. 630-637, April 2010.
6. A. Montone, M. D. Santambrogio, D. Sciuto, S. Ogrenci Memik, "Placement and Floorplanning in Dynamically Reconfigurable FPGAs", ACM Transactions on Reconfigurable Technology and Systems (TRETS), Vol. 4(1), 2010.

7. F. Redaelli, M. D. Santambrogio, S. Ogrenci Memik, "An ILP formulation for the Task Graph Scheduling Problem tailored to bi-dimensional Reconfigurable Architectures", *International Journal on Reconfigurable Computing (IJRC)*, Vol. 2009, pp. 1-12, 2009.
8. J. Long, H. Zhou, S. Ogrenci Memik, "EBOARST: An Efficient Edge-Based Obstacle-Avoiding Rectilinear Steiner Tree Construction Algorithm", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 12, pp. 2169-2182, December 2008.
9. S. Ogrenci Memik, N. Bellas, S. Mondal, "Pre-synthesis Area Estimation of Reconfigurable Streaming Accelerators", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 11, pp. 2027-2038, November 2008.
10. R. Mukherjee, S. Liu, S. Ogrenci Memik, S. Mondal, "A High-Level Clustering Algorithm Targeting Dual Vdd FPGAs", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 13, Issue 4, pp. 57-76, September 2008.
11. J. Long, S. Ogrenci Memik, G. Memik, R. Mukherjee, "Thermal Monitoring Mechanisms for Chip Multiprocessors", *ACM Transactions on Architecture and Code Optimization (TACO)*, Vol. 5, Issue 2, pp. 9-41, August 2008.
12. S. Ogrenci Memik, R. Mukherjee, M. Ni, J. Long, "Optimizing Thermal Sensor Allocation for Microprocessors", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 27, No. 3, pp. 516—527, March 2008.
13. R. Mukherjee, S. Ogrenci Memik, "An Integrated Approach to Thermal Management in High-Level Synthesis", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 14, No. 1, pp. 1165—1174, November 2006.
14. E. Kursun, R. Mukherjee, S. Ogrenci Memik, "Early Quality Assessment for Low Power Behavioral Synthesis", *Journal of Low Power Electronics (JOLPE)*, Vol. 1, No. 3, pp. 273—285, December 2005.
15. A. Srivastava, S. Ogrenci Memik, B.K. Choi, M. Sarrafzadeh, "On Effective Slack Management in Post-Scheduling Phase", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol. 24, No. 4, April 2005.
16. S. Ogrenci Memik, R. Kastner, E. Bozorgzadeh, M. Sarrafzadeh, "A Scheduling Algorithm for Optimization and Planning in High-level Synthesis", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 10, No. 1, January 2005.
17. E. Bozorgzadeh, S. Ogrenci Memik, X. Yang, M. Sarrafzadeh, "Routability-driven Packing: Metrics and Algorithms for Cluster-based FPGAs", *Journal of Circuits, Systems, and Computers (JCSC)*, Vol. 13, No. 1, February 2004.
18. S. Ogrenci Memik, A. K. Katsaggelos, M. Sarrafzadeh, "FPGA Implementation and Analysis of an Iterative Image Restoration Algorithm", *IEEE Transactions on Computers*, Vol. 52 No.3, March 2003.
19. R. Kastner, A. Kaplan, S. Ogrenci Memik, E. Bozorgzadeh, "Instruction Generation for Hybrid Reconfigurable Systems", *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 7, No. 4, October 2002.
20. Ranjan, K. Bazargan, S. Ogrenci, M. Sarrafzadeh, "Fast Floorplanning for Effective Prediction and Construction", *IEEE Transactions on VLSI (TVLSI)*, Vol. 9, No. 2, April 2001.

### **Refereed Conference/Workshop Publications**

1. S. Liu, S. Ogrenci Memik, Y. Ismail, "A Comprehensive Tapered Buffer Optimization Algorithm for Unified Design Metrics", *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 15-18, 2011, Rio de Janeiro, Brazil.
2. A. A. Del Barrio Garcia, S. Ogrenci Memik, M. C. Molina, J. M. Mendias, R. Hermida, "Power Optimization in Heterogenous Datapaths", *Design, Automation and Test in Europe (DATE)*, 14-18 March, 2011, Grenoble, France.
3. S. Liu, B. Leung, A. Neckar, S. Ogrenci Memik, G. Memik, N. Hardavellas, "Hardware/Software Techniques for DRAM Thermal Management", *IEEE International Symposium on High-Performance Computer Architecture Conference (HPCA)*, February 14-16, 2011, San Antonio, TX.
4. J. Long, G. Klock, C. Zhou, S. Ogrenci Memik, M. Grayson, "IOTA: Towards an Integrated On-chip Thermocouple Array", *International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, October, 2010, Barcelona, Spain.
5. B. Leung, C. Wu, S. Ogrenci Memik, S. Mehrotra, "An Interior Point Optimization Solver for Real Time Inter-Frame Collision Detection: Exploring Resource-Accuracy-Platform Tradeoffs", *International Conference on Field Programmable Logic and Its Applications (FPL)*, August 31-September 2, 2010, Milan, Italy.
6. J. Long, S. Ogrenci Memik, "A framework for optimizing thermoelectric active cooling systems", *IEEE/ACM Design Automation Conference (DAC)*, July 13-18, 2010, Anaheim, CA.
7. M. Ni, S. Ogrenci Memik, "A Revisit to the Primal-Dual Based Clock Skew Scheduling Algorithm", *International Symposium on Quality Electronic Design (ISQED)*, March 22-24, 2010, San Jose, CA

8. A. A. Del Barrio Garcia, M. C. Molina, J. M. Mendias, R. Hermida, S. Ogrenci Memik, "Using Speculative Functional Units in High Level Synthesis", Design, Automation and Test in Europe (DATE), March 8-12, 2010, Dresden, Germany
9. J. Long, S. Ogrenci Memik, M. Grayson, "Optimization of Thin-film Thermoelectric Cooler based On-chip Active Cooling System", Design, Automation and Test in Europe (DATE), March 8-12, 2010, Dresden, Germany
10. J. Long, S. Ogrenci Memik, "Optimization of the Bias Current Network for Accurate On-Chip Thermal Monitoring", (Interactive Presentation) Design, Automation and Test in Europe (DATE), March 8-12, 2010, Dresden, Germany
11. J. Long, S. Ogrenci Memik, "Inversed Temperature Dependence Aware Clock Skew Scheduling for Sequential Circuits", (Interactive Presentation) Design, Automation and Test in Europe (DATE), March 8-12, 2010, Dresden, Germany
12. F. Redaelli, M. D. Santambrogio, V. Rana, S. Ogrenci Memik, "Scheduling and 2D Placement Heuristics for Partially Reconfigurable Systems", International Conference on Field-Programmable Technology (FPT), December 9-11 2009, Sydney, Australia.
13. C.-H. Wu, S. Ogrenci Memik, S. Mehrotra, "FPGA Implementation of the Interior-Point Algorithm for Linear Programming with Applications to Collision Detection", (Short Paper) IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April 2009, Napa, CA
14. B. Leung, Y. Pan, C. Schroeder, S. Ogrenci Memik, G. Memik, and M. Hartmann, "Towards an "Early Neural Circuit Simulator": An FPGA Implementation of Processing In the Rat Whisker System", International Conference on Field-Programmable Logic and Applications (FPL), September 9-11, 2008, Heidelberg, Germany
15. S. Liu, S. Ogrenci Memik, Y. Zhang, G. Memik, "An Approach for Adaptive DRAM Temperature and Power Management", in Proc. ACM International Conference on Supercomputing (ICS), June 7-12, 2008, Kos, Greece
16. J. Long, S. Ogrenci Memik, "Automated Design of Self-Adjusting Pipelines", in Proc. IEEE/ACM Design Automation Conference (DAC), June 8-13, 2008, Anaheim, CA
17. M. Ni, S. Ogrenci Memik, "Leakage Power-Aware Clock Skew Scheduling: Converting Stolen Time into Leakage Power Reduction", in Proc. IEEE/ACM Design Automation Conference (DAC), June 8-13 2008, Anaheim, CA
18. S. Liu, S. Ogrenci Memik, Y. Zhang, G. Memik, "A Power and Temperature Aware DRAM Architecture", in Proc. IEEE/ACM Design Automation Conference (DAC), June 8-13 2008, Anaheim, CA
19. J. Long, H. Zhou, S. Ogrenci Memik, "An O(nlogn) Edge-Based Algorithm for Obstacle-Avoiding Rectilinear Steiner Tree Construction", in Proc. ACM International Symposium on Physical Design (ISPD), April 13-16, 2008, Portland, OR
20. M. Santambrogio, M. Gianni, S. Ogrenci Memik, "Managing Reconfigurable Resources in Heterogeneous Cores using Portable Pre-Synthesized Templates", in Proc. International Symposium on System-on-Chip, November 19-21, 2007, Tampere, Finland
21. M. Ni, S. Ogrenci Memik, "Early Planning for Clock Skew Scheduling during Register Binding", in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 5-8, 2007, San Jose, CA
22. J. Long, J. Ku, S. Ogrenci Memik, Y. Ismail, "A Self-Adjusting Clock Tree Architecture to Cope with Temperature Variations", in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 5-8, 2007, San Jose, CA **[IEEE/ACM William J. McCalla ICCAD Best Paper Award Finalist]**
23. M. Santambrogio, V. Rana, S. Ogrenci Memik, U. Acar, D. Scuito, "A Novel SoC Design Methodology Combining Adaptive Software and Reconfigurable Hardware", in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 5-8, 2007, San Jose, CA
24. M. Ni, S. Ogrenci Memik, "Self-Heating-Aware Optimal Wire-Sizing Under Elmore Delay Model", in Proc. Design, Automation and Test in Europe (DATE), 16-20 April, 2007, Niece, France
25. Marco Santambrogio, Vincenzo Rana, Seda Ogrenci Memik and Donatella Sciuto, "Combining Hardware Reconfiguration and Adaptive Computation for a Novel SoC Design Methodology", in Proc. IEEE International Conference on Field-Programmable Technology (FPT), December 13-15, Bangkok, Thailand
26. R. Mukherjee, S. Mondal, S. Ogrenci Memik, "Thermal Sensor Allocation and Placement for Reconfigurable Systems", in Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 5-9 2006, San Jose, CA
27. R. Mukherjee, S. Ogrenci Memik, "Physical Aware Frequency Selection for Dynamic Thermal Management in Multi-Core Systems", in Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 5-9 2006, San Jose, CA
28. M. Ni, S. Ogrenci Memik, "Thermal-Induced Leakage Power Optimization by Redundant Resource Allocation", in Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 5-9 2006, San Jose, CA
29. S. Ogrenci Memik, M. Santambrogio, G. Agosta, "Adaptive Metrics for System-Level Functional Partitioning", in Proc. Forum on Specification and Design Languages (FDL), September 19-22 2006, Darmstadt, Germany

30. S. Mondal, S. Ogrenç Memik, N. Bellas, "Pre-Synthesis Area Estimation of Reconfigurable Streaming Accelerators", in Proc. International Conference on Field Programmable Logic and Applications (FPL), August 28-30 2006, Madrid, Spain
31. R. Mukherjee, S. Ogrenç Memik, "Systematic Temperature Sensor Allocation and Placement for Microprocessors", in Proc. IEEE/ACM Design Automation Conference (DAC), July 24-28, 2006, San Francisco, CA
32. R. Mukherjee, S. Mondal, S. Ogrenç Memik, "A Sensor Distribution Algorithm for FPGAs with Minimal Dynamic Reconfiguration Overhead", in Proc. International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), June 26-29, 2006, Las Vegas, NV
33. S. Mondal, R. Mukherjee, S. Ogrenç Memik, "Fine-Grain Thermal Profiling and Sensor Insertion for FPGAs", in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), May 21-24 2006, Kos, Greece
34. S. Mondal, S. Ogrenç Memik, N. Bellas, "Pre-synthesis Queue Size Estimation of Streaming Data Flow Graphs (Poster Presentation, 2-page extended abstract in the proceedings), IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April 24-26, 2006, Napa, CA
35. D. Nguyen, G. Memik, S. Ogrenç Memik, and A. Choudhary, "Real-Time Feature Extraction for High Speed Networks", in Proc. International Conference on Field Programmable Logic and Applications (FPL), August 24-26 2005, Tampere, Finland
36. R. Mukherjee, S. Ogrenç Memik, G. Memik, "Peak Temperature Control and Leakage Reduction During Binding in High-Level Synthesis", in Proc. ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 8-10 2005, San Diego, CA
37. R. Mukherjee, S. Ogrenç Memik, G. Memik, "Temperature-aware Resource Allocation and Binding in High-Level Synthesis", in Proc. IEEE/ACM Design Automation Conference (DAC), June 13-17 2005, Anaheim, CA **[Best Paper Award Nomination]**
38. S. Mondal, S. Ogrenç Memik, "A Low Power FPGA Routing Architecture", in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), May 23-26 2005, Kobe, Japan.
39. S. Mondal, S. Ogrenç Memik, "Fine-Grain Leakage Optimization in SRAM based FPGAs", in Proc. Great Lakes Symposium on VLSI (GLSVLSI), April 17-19, Chicago, IL.
40. R. Jafari, S. Ogrenç Memik, M. Sarrafzadeh, "Quick Reconfiguration in Clustered Micro-Sequencer", International Parallel and Distributed Processing Symposium (IPDPS), in Proc. Reconfigurable Architectures Workshop (RAW), April 4-5 2005, Denver, CO
41. S. Mondal, S. Ogrenç Memik, D. Das, "Hierarchical LUT Structures for Leakage Power Reduction" Poster Presentation, ACM International Symposium on Field Programmable Gate Arrays (FPGA), February 20-22 2005, Monterey, CA
42. S. Mondal, S. Ogrenç Memik, "Resource Sharing in Pipelined CDFG Synthesis", in Proc. IEEE/ACM Asia-South Pacific Design Automation Conference (ASP-DAC), January 18-21, Shanghai, China
43. R. Mukherjee, S. Ogrenç Memik, "Evaluation of Dual Vdd Fabrics for Low Power FPGAs", in Proc. IEEE/ACM Asia-South Pacific Design Automation Conference (ASP-DAC), January 18-21, Shanghai, China
44. R. Mukherjee, S. Ogrenç Memik, "Power-driven Design Partitioning", in Proc. International Conference on Field-Programmable Logic and Its Applications (FPL), August 30 –September 1 2004, Antwerp, Belgium
45. R. Mukherjee, S. Ogrenç Memik, "Power Management for FPGAs: Power-driven Design Partitioning" (Poster Presentation, 2-page extended abstract included in the proceedings), IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April 2004, Napa, CA
46. A. Srivastava, S. Ogrenç Memik, B. K. Choi, M. Sarrafzadeh, "Achieving Design Closure through Delay Relaxation Parameter", in Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 2003, San Jose, CA
47. S. Ogrenç Memik, G. Memik, R. Jafari, E. Kursun, "Global Resource Sharing for Synthesis of Control Data Flow Graphs on FPGAs", in Proc. IEEE/ACM Design Automation Conference (DAC), June 2003, Anaheim, CA
48. S. Ogrenç Memik, F. Fallah, "Accelerated SAT-based Scheduling of Control/Data Flow Graphs", in Proc. International Conference on Computer Design (ICCD), September 2002, Freiburg, Germany
49. E. Kursun, A. Srivastava, S. Ogrenç Memik, M. Sarrafzadeh, "Early Evaluation Techniques for Low Power Binding", in Proc. ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), August 2002, Monterey, CA
50. E. Bozorgzadeh, S. Ogrenç Memik, R. Kastner, M. Sarrafzadeh, "Pattern Selection: Customized Block Allocation for Domain-Specific Programmable Systems", in Proc. International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA), June 2002, Las Vegas, NV
51. S. Ogrenç Memik, F. Fallah, "Accelerated Boolean Satisfiability-Based Scheduling for High-Level Synthesis", IEEE/ACM International Workshop on Logic & Synthesis (IWLS), June 2002, New Orleans, LA.

52. G. Memik, S. Ogreneci Memik, W. H. Mangione-Smith, "Design and Analysis of a Layer Seven Network Processor Accelerator Using Reconfigurable Logic", in Proc. IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April 2002, Napa, CA.
53. E. Bozorgzadeh, R. Kastner, S. Ogreneci Memik and M. Sarrafzadeh, "Pattern Selection in Programmable Systems" (poster presentation), ACM International Symposium on Field Programmable Gate Arrays (FPGA), February 2002, Monterey, CA.
54. S. Ogreneci Memik, E. Bozorgzadeh, R. Kastner, M. Sarrafzadeh, "A Super-Scheduler for Embedded Reconfigurable Systems", in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 2001, San Jose, CA
55. R. Kastner, S. Ogreneci Memik, E. Bozorgzadeh, M. Sarrafzadeh, "Instruction Generation for Hybrid Reconfigurable Systems", in Proc. IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 2001, San Jose, CA
56. K. Bazargan, S. Ogreneci, M. Sarrafzadeh, "Integrating Scheduling and Physical Design into a Coherent Compilation Cycle for Reconfigurable Computing Architectures", in Proc. IEEE/ACM Design Automation Conference (DAC), June 2001, Las Vegas, NV [Best Paper Award Nomination]
57. S. Ogreneci Memik, E. Bozorgzadeh, R. Kastner, M. Sarrafzadeh, "SPS: A Strategically Programmable System", International Parallel and Distributed Processing Symposium (IPDPS), Reconfigurable Architectures Workshop (RAW), April 2001, San Francisco, CA
58. E. Bozorgzadeh, S. Ogreneci Memik, M. Sarrafzadeh, "RPACK: Routability-Driven Packing for Cluster-Based FPGAs", in Proc. Asia-South Pacific Design Automation Conference (ASP-DAC), January 2001, Yokohama, Japan
59. S. Ogreneci, K. Bazargan, M. Sarrafzadeh, "Image Analysis and Partitioning for FPGA Mapping", in Proc. IEEE Workshop on Signal Processing Systems (SiPS), October 2000, Lafayette, LA
60. K. Bazargan, R. Kastner, S. Ogreneci, M. Sarrafzadeh, "A C to Hardware/Software Compiler", (Poster Presentation, 2-page extended abstract included in the proceedings), IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), April 2000, Napa Valley, CA
61. S. Ogreneci, A. K. Katsaggelos, M. Sarrafzadeh, "FPGA Implementation and Analysis of Image Restoration" (poster presentation), ACM International Symposium on Field Programmable Gate Arrays (FPGA), February 2000, Monterey, CA

## Book Chapters

62. E. Bozorgzadeh, R. Kastner, S. Ogreneci Memik, M. Sarrafzadeh, "Strategically Programmable Systems", The Computer Engineering Handbook, CRC Press, December 2001
63. E. Bozorgzadeh, A. Kaplan, R. Kastner, S. Ogreneci Memik, M. Sarrafzadeh, "Optimization for Reconfigurable Systems Using Hierarchical Abstraction", J. Cong and J. R. Shinnerl (editors), Multilevel Optimization and VLSICAD, Kluwer Academic Publishers, Boston, 2002

## GRANTS

### Research Grants

1. "SHF: Small: Thermal-Aware High-Performance DRAM Architectures in Multicore Technologies", NSF CCF-0916746; 09/2009-08/2012, \$450,000; PI (with co-PI Gokhan Memik).
2. "Thermal Monitoring Infrastructures for Multi-core Systems"; Semiconductor Research Corporation (SRC) Grant No. G00639; 09/2007 (non-expiring), \$40,000; PI
3. "Computational and Hardware Models of Active Sensing Behaviors"; NSF IIS-0613568; 09/2006 – 09/2009; \$350,000; co-PI, with Mitra Hartmann (PI) and Gokhan Memik
4. "Self-Adjusting Architectures/Circuits for Improved Performance and Reduced Design Complexity"; NSF CCF-0541337; 04/2006 – 04/2009; \$450,000; co-PI, with Gokhan Memik (PI), Russ Joseph, and Yehea Ismail
5. "CAREER: Thermal-Aware Synthesis of Embedded Processors"; NSF CNS-0546305 (NSF CAREER Award); 03/2006 – 02/2011; \$400,000; PI
6. "Collaborative Research: High-Performance Techniques, Design and Implementation of Software Infrastructure for Change Detection and Mining"; NSF IIS-0536994; 09/2005 – 09/2008; this is a collaborative work with Indiana University; Northwestern amount: \$514,450; co-PI, with Alok Choudhary (PI), Aggelos Katsaggelos, Ying Wu, and Gokhan Memik
7. "Collaborative Research: Ultra-scalable system software and tools for data-intensive computing"; NSF CCF-0444405; 10/2004 – 09/2008; this is a collaborative work with Pennsylvania State University and DePaul University - Northwestern amount: \$259,521; co-PI, with Alok Choudhary (PI) and Gokhan Memik

8. Alumnae of Northwestern Research Initiation Grant, \$3,000; PI.
9. Motorola Undergraduate Research Grant to support the research of undergraduate student Elaine Jen.
10. NSF REU: Modeling Timing Variation under Process Variation during High-level Synthesis
11. Equipment donation from Xilinx Inc. (FPGA development boards and design software worth \$10,000)

### **Educational Grants**

12. Equipment Donation from Altera Inc. (FPGA development boards and design software worth \$6,000)
13. “Design and Prototyping Laboratory for Computer Engineering Curriculum”; Internal Grant, Murphy Society; 09/2007-08/2008; \$25,000; Primary Instructor, with Yehea Ismail
14. “Proposal for Modern Circuits and Signals Laboratory Development”; Internal Grant, Murphy Society; 11/2005 – 11/2006; \$45,000; with Lawrence J. Henschen (PI), Robert Dick, Yehea Ismail, Mary Phillips, Russ Joseph, Gokhan Memik, Alan Sahakian, and Chi-Haur Wu

## **PROFESSIONAL ACTIVITIES**

### **Service**

- Editorial Boards
  - IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Associate Editor, Jan. 2007-ongoing
- Organizing Committee
  - Publicity Co-Chair, International Symposium on Field Programmable Logic and Its Applications (FPL) 2010
  - Local Arrangements Co-Chair for the Great Lakes Symposium on VLSI (GLSVLSI) 2005
- Technical Program Committees
  - Design Automation Track Chair, Asia South Pacific Quality Electronic Design (ASQED) 2010 - 2012
  - VLSI-CAD Track Co-Chair International Symposium on VLSI (ISVLSI) 2009
  - *System Design Track Chair*; IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2007)
  - *High-Level Synthesis Track Chair*; IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2006)
  - TPC Member: IEEE/ACM International Conference on Computer Aided Design (ICCAD) 2004-2007, 2011
  - TPC Member: International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC) 2011
  - TPC Member: International Symposium on Field Programmable Logic and Its Applications (FPL) 2005-2012
  - TPC Member: Reconfigurable Architectures Workshop (RAW) 2008-2010
  - TPC Member: Great Lakes Symposium on VLSI (GLSVLSI) 2004-2009
  - TPC Member: Design, Automation and Test in Europe (DATE) 2006
  - TPC Member: Applied Reconfigurable Computing (ARC) Workshop (ARC) 2007-2011
  - TPC Member: Southern Conference on Programmable Logic (SPL) 2008-2011
- Chaired sessions at ICCAD, FPL, ISCAS.
- Served on three NSF Panels between 2003-present
- Reviewer for over 30 conferences and journals, i.e., every major conference and journal in CAD, Reconfigurable Computing, and VLSI.

### **Invited Talks**

1. “Thermal Aware Design and Optimizations for High Performance Integrated Circuits”, Electrical and Computer Engineering Department, Illinois Institute of Technology, September 16, 2011.
2. “Thermal Issues in High Performance Integrated Circuits”, Electrical Engineering Department, Politecnico di Milano, Milan, Italy, May 20, 2010.
3. “Tools for Optimization of Active Cooling Systems for MPSoCs”, Workshop on Compiler Assisted System-on-Chip Assembly, Grenoble, France, October 11, 2009.
4. “Design Automation for Thermal Effects and Other Sources of Variation: An Overview”, School of Engineering and Sciences, Sabanci University, Istanbul, Turkey, September 9, 2009.
5. “Thermal-Aware Design”, Integrated Systems Center, École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, September 10, 2008.

6. "Design and Optimization of Thermal Monitoring Infrastructures", IMEC, Leuven, Belgium, September 5, 2008.
7. "Thermal-Aware Design", Electrical and Computer Engineering Department, University of Wisconsin-Madison, February 29, 2008
8. "Thermal-Aware Synthesis", Strategic CAD Labs, Intel Inc, November 20, 2005, Hillsboro, OR
9. "An Architecture Exploration and Synthesis Framework for Reconfigurable Fabrics", Center for Embedded Hardware Systems Research, Motorola Inc., February 15, 2005, Schaumburg, IL.
10. "Overview of Embedded and Hybrid Systems Research", Privacy and Security Technologies Lab, Motorola Inc., July 28, 2004, Schaumburg, IL
11. "CAD Tools and Architectures for Low Power FPGAs", Xilinx Inc., February 20, 2004, San Jose, CA

## ADVISING, TEACHING, AND UNIVERSITY SERVICE

### Current Graduate Students

Brian Leung, PhD, expected graduation: 2012

Dawei Li, PhD student

Kaicheng Zhang (co-Advisor: Gokhan Memik), PhD student

### Alumni

- PhD
  - Song Liu, August 2011. Thesis: Architectural and OS-Level Performance and Thermal Optimizations for DRAM Systems. Current Position: Facebook, Inc.
  - Jieyi Long, March 2010. Thesis: Design of Thermal Monitoring Infrastructures and Thermal Optimizations for High Performance Chips. Current Position: Magma Design Automation.
  - Min Ni, March 2009. Thesis: Thermal Aware and Low Power Optimizations for VLSI Synthesis. Current Position: Synopsys, Inc.
  - Somsubhra Mondal, June 2007. Thesis: Architectural Optimizations and Synthesis Tools for Improved Energy Efficiency and Faster Design Closure for FPGAs. Current position: Ronin Capital
  - Rajarshi Mukherjee, June 2006. Thesis: Thermal-aware design and analysis techniques for integrated circuits and high-performance microprocessor systems. Current position: Mentor Graphics, Inc.
- MS
  - Ryan Cortez 2010 (Project), Chih-Hung Wu 2009 (Thesis).

### Thesis Defense Committees

- PhD defense committee
  - Alberto del Barrio Garcia (external member, Complutense Universidad de Madrid), Song Liu (chair), Jieyi Long (chair), Min Ni (chair), Somshubra Mondal (chair), Rajarshi Mukherjee (chair), Yan Pan, Alex Shye, Me Keng, Ruiming Chen, Zhenyu Gu, Ja Chun Ku, DiaaEldin Khalil, Nikos Liveris, Serkan Ozdemir, Ahmed Shebaita, Jia Wang, Joseph Zambreno, David Zaretsky
- MS committee
  - Utku Pamuksuz, Ryan Cortez (chair), Chih-Hung Wu (chair), Anitha Mohan, David Nguyen, Seunghoon Kim, Sanghamitra Roy

### University/Department Committees

- Chair of the Publicity, Alumni, and Industrial Relations Committee (2011 – present)
- Undergraduate Recruiting Committee (2006-present)
- Chair of the Computer Engineering Undergraduate Curriculum Committee (2008-2010)
- Computer Engineering Undergraduate Curriculum Committee (2003-ongoing)
- McCormick School of Engineering Curriculum Committee (2009-2010)
- Computer Science Undergraduate Curriculum Committee (2006-2007 academic year)