

Short Papers

Optimum Positioning of Interleaved Repeaters in Bidirectional Buses

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Abstract—It is shown in this paper that the optimum position of interleaved repeaters for minimum delay and noise is not the midpoint as commonly practiced. A closed-form solution for the optimum position has been derived in this paper and verified by simulation. Bidirectional buses with the optimum interleaved repeater position are compared to commonly used bidirectional buses and shown to provide an improvement greater than 50% in the propagation delay and bit-rate per unit area. The area of the induced noise pulse on victim lines is shown to be zero indicating that the aggressor lines are virtually static with the optimum repeater position. The presented optimum repeater positioning also provides lower noise pulse amplitude as well as lower sensitivity of propagation delay and noise pulse peak to segment length variation, compared to commonly used midway repeater positioning.

Index Terms—Bidirectional buses, coupling capacitance, delay, interleaved repeaters, noise, on-chip buses, repeater insertion, signal integrity.

I. INTRODUCTION

With the continuous scaling of technology, increased die area and faster clock speeds, the delay and noise of on-chip buses are becoming one of the main bottlenecks in current integrated circuits. The delay and noise through a long bus is a strong function of the coupling capacitance between the wires. Especially detrimental to delay is the Miller-like effect when adjacent wires simultaneously switch in opposite directions.

As the technology is scaled, the lateral component of interconnect capacitance (coupling capacitance) grows to dominate the total interconnect capacitance due to reduction in wire pitch and the increase in the interconnects' aspect ratio. It is shown in [1] and [2], that in recent deep submicron (DSM) technologies, the lateral interconnect capacitance components can be from three to five times as much as the vertical component. As can be seen from Fig. 1, avoiding these delay and noise problems would involve drastically increased wire spacing or extensive shielding [3]. However, studies show that current very large scale integration (VLSI) designs tend to be interconnect-limited for die area, which increase the penalty for spacing and shielding. Thus, extensive research has been conducted for more complex strategies to minimize degradation in interconnect performance and noise due to coupling capacitance, e.g., [4]–[19].

In current bus-design methodologies, designers interleave the position of the repeaters along each line to further reduce the delay due to coupling. A repeater on a unidirectional or a bidirectional bus line is usually positioned exactly midway between the positions of two consecutive repeaters on the adjacent bus line as shown in Fig. 2. This placement reduces the worst-case crosstalk delay by 50% compared to the delay of a bus without interleaved repeaters. This reduction is due

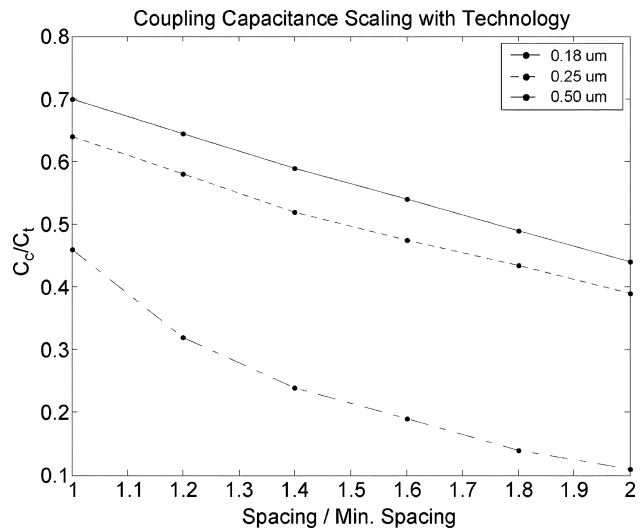


Fig. 1. Coupling capacitance scaling with technology [3].

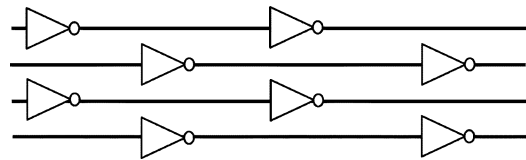


Fig. 2. Interleaved repeaters on a bus.

to the fact that when half of the aggressor line switches in a certain direction, the other half switches in the opposite direction, significantly reducing the net coupling capacitance. Hence, the effective coupling capacitance between the aggressor and victim lines is reduced, leading to a reduction in both the propagation delay component due to crosstalk and the induced noise on the victim line.

The rest of the paper is organized as follows. In Section II, the optimum interleaved repeater position for minimum propagation delay is analytically derived, which will also be shown to provide zero noise pulse area. The amplitude of the noise pulse as well as its sensitivity to segment length variation is also presented. Extensive simulation results to support all analytical results are provided as well. A comparison in propagation delay and noise is also performed between buses with optimal and midway repeater positions. Section III provides simulation results showing the effect of optimum positioning of interleaved repeaters in *bidirectional* buses on the propagation delay, the noise pulse area and peak, and the sensitivity to segment length variation. Also in Section III, the performance of bidirectional buses with the optimal interleaved repeater positions, derived in Section II, is compared to that of other bidirectional buses commonly used in current integrated circuits. Finally, Section IV presents the conclusion.

II. OPTIMUM INTERLEAVED REPEATER POSITION

In this section, the variation of propagation delay and noise with the interleaved repeater position is investigated. In Section II-A, the optimum interleaved repeater position for minimum propagation delay is derived. The sensitivity of the propagation delay to segment length is

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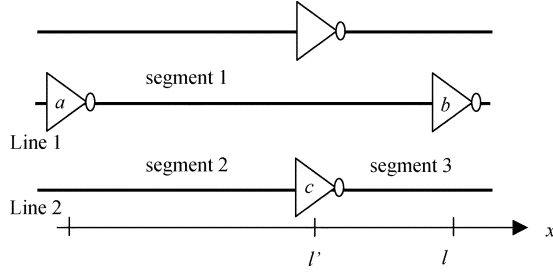


Fig. 3. Two adjacent bus lines with interleaved repeaters.

then considered in Section II-B. The optimum interleaved repeater position for minimum noise pulse area is derived in Section II-C. Simulation results are presented to support all the analytical conclusions and compare the optimal positioning scheme, obtained in Sections II-A and II-C, to the commonly used midway-positioning scheme. Section II-F will finally discuss the practical issues of implementing the optimal interleaved repeater schemes in unidirectional and bidirectional buses.

A. Optimum Interleaved Repeater Position for Minimal Propagation Delay

It is commonly and erroneously assumed that the optimum position of interleaved repeaters for minimum delay is the interconnect segment's midpoint. However, the optimum position for minimum delay, as is shown in this section, should be downstream of the segment's midpoint. This result can be explained by noting that the aim of interleaving the repeaters is to divide each segment into two parts coupled to segments switching in opposite directions. If the two parts have an equal share in the overall delay due to coupling, the total delay due to coupling can be cancelled. However, the coupling capacitance at the end of the line is driven by more resistance than that at the beginning of the line, and contributes more to the delay. Therefore, the point at which the capacitance of each segment part equally contributes to the delay, will be downstream of the center of the segment.

Consider a three-line bus with interleaved repeaters as shown in Fig. 3. Repeaters are inserted along the lines to divide the lines into segments of length l . Repeaters on a line are positioned at a distance l' relative to the adjacent line repeaters. In order to get the delay at the end of segment 1 (between the output of inverter a and the input of inverter b), we have to consider the coupling from segment 2 (right before inverter c on line 2) and segment 3 (right after inverter c on line 2). Thus, the delay, t_p , of segment 1 can be expressed by a scaled Elmore time constant, representing the 10%–90% transition time, which be formulated as

$$t_p = 2.3 \times \left\{ \int_0^{l'} (R_{inv} + rx) \cdot (c_g + \alpha_{12} \cdot c_c) dx + \int_{l'}^l (R_{inv} + rx) \cdot (c_g + \alpha_{13} \cdot c_c) dx + (rl + R_{inv}) C_{inv} \right\} \quad (1)$$

where r is the line's resistance per unit length, c_g is the line's vertical capacitance component per unit length and c_c is the line's lateral capacitance (from both sides) component per unit length. R_{inv} and C_{inv} are the repeater's output resistance and input capacitance, respectively. α_{12} is the switching activity coefficient between segments 1 and 2, while α_{13} is the switching activity coefficient between segments 1 and 3. α_{12}

TABLE I
SWITCHING ACTIVITY COEFFICIENTS FOR DIFFERENT WIRE SWITCHING CONDITIONS

| Switching Case | α_{12} | α_{13} |
|--|---------------|---------------|
| 1. No activity on line 2 and 3 | 1 | 1 |
| 2. Segments 1 and 2 are switching in opposite directions | 2 | 0 |
| 3. Segments 1 and 2 are switching in the same direction | 0 | 2 |

and α_{13} take the values shown in Table I. Performing the integration in (1)

$$t_p = 2.3 \times \left\{ (rl + R_{inv}) C_{inv} + R_{inv} c_g l + \frac{rc_g l^2}{2} + \frac{rc_c}{2} [\alpha_{12} l'^2 + \alpha_{13} (l^2 - l'^2)] + R_{inv} c_c [\alpha_{12} l' + \alpha_{13} (l - l')] \right\}. \quad (2)$$

Equation (2) can be rewritten as

$$t_p = t_{p0} + t_{pc} \left\{ [\alpha_{12} \beta^2 + \alpha_{13} (1 - \beta^2)] + 2\eta_r [\alpha_{12} \beta + \alpha_{13} (1 - \beta)] \right\} \quad (3)$$

where

$$t_{p0} = 2.3 \times \left\{ (rl + R_{inv}) C_{inv} + R_{inv} c_g l + \frac{rc_g l^2}{2} \right\} \quad (4)$$

$$t_{pc} = 2.3 \times \frac{rc_c l^2}{2} \quad (5)$$

$$\eta_r = \frac{R_{inv}}{rl} \quad (6)$$

$$\beta = \frac{l'}{l}, \quad 0 < \beta \leq 1. \quad (7)$$

There are three possible switching scenarios for the three lines shown in Fig. 3 if the two external lines switch similarly. This results in the switching activity coefficients α_{12} and α_{13} listed in Table I. Each of these cases has a different propagation delay equation as given in

case 1 :

$$t_{p11} = t_{p0} + t_{pc} \{1 + 2\eta_r\}$$

case 2 :

$$t_{p20} = t_{p0} + t_{pc} \{2\beta^2 + 4\eta_r \beta\}$$

case 3 :

$$t_{p02} = t_{p0} + t_{pc} \{2(1 - \beta^2) + 4\eta_r (1 - \beta)\}. \quad (8)$$

The worst-case propagation delay at any given interleaved repeater position will thus be

$$t_p(\beta) = \max(t_{p11}, t_{p20}, t_{p02}). \quad (9)$$

Based on (9), the problem can be defined as follows. It is required to find the optimum relative position ratio, β_{opt} , that minimizes the worst-case propagation delay in each of the switching possibilities of lines 1 and 2.

Closely examining (8), there exists a certain value β_{opt} , such that when $\beta > \beta_{opt}$ then $t_{p20} > t_{p11}$ and $t_{p02} < t_{p11}$, while when $\beta < \beta_{opt}$ then $t_{p20} < t_{p11}$ and $t_{p02} > t_{p11}$. Thus,

$$\text{at } \beta = \beta_{opt} \quad t_{p20} = t_{p02} = t_{p11}. \quad (10)$$

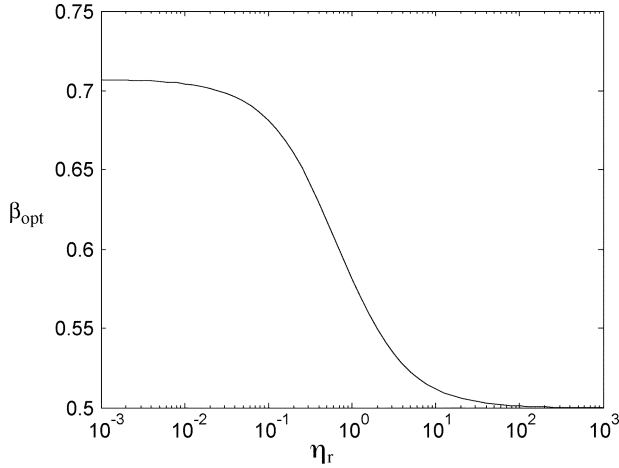


Fig. 4. Variation of β_{opt} with the resistance ratio η_r .

Substituting from (8) into (10) gives

$$1 + 2\eta_r = 2\beta_{opt}^2 + 4\eta_r\beta_{opt}. \quad (11)$$

Solving (11) yields

$$\beta_{opt} = 0.5 \times \left[\sqrt{(2\eta_r + 1)^2 + 1} - 2\eta_r \right] \quad (12)$$

$$\frac{1}{2} < \beta_{opt} < \frac{1}{\sqrt{2}}. \quad (13)$$

Equation (12) shows that the optimal relative position ratio β_{opt} depends only on the ratio of the repeater's output resistance to the interconnect's resistance η_r and varies from 0.5 to 0.707. When the inverter output resistance R_{inv} dominates the line resistance rl , the resistance ratio η_r is very large and the propagation delay varies linearly with β , as shown in (3). This makes β_{opt} approach 0.5. At the other extreme, when the line resistance dominates the inverter output resistance, the resistive ratio η_r approaches zero and the propagation delay varies quadratically with β . This makes β_{opt} approach 0.707. The variation of β_{opt} with η_r expressed by (12) is illustrated in Fig. 4.

In current DSM technologies, the line resistance is usually comparable or higher than the repeater's output resistance. Thus, the optimum relative position ratio, β_{opt} will be closer to 0.707, rather than 0.5 as commonly assumed. Substituting from (12) in (9), the optimum (minimal) propagation delay will thus be

$$t_{p,opt} = t_{p0} + t_{pc}\{1 + 2\eta_r\}. \quad (14)$$

The optimal propagation delay $t_{p,opt}$ given by (14) is exactly the same as the propagation delay, t_{p11} in (8), when line 2 has no activity. Thus, placing the interleaved repeaters at the optimal position ($\beta_{opt,l}$) causes adjacent lines to appear as virtual static lines independent of their switching condition.

If the repeaters on a line are positioned exactly midway between any two repeaters on the adjacent line, i.e. $\beta = 0.5$, this will lead to a nonoptimal propagation delay which can be obtained by substituting $\beta = 0.5$ in (9).

$$t_{p,mid} = t_{p0} + t_{pc}\{1.5 + 2\eta_r\}. \quad (15)$$

This delay is higher than the optimal delay by

$$\frac{\Delta t_p}{t_{p,opt}} = \frac{0.5 \times t_{pc}}{t_{p0} + t_{pc}\{1 + 2\eta_r\}} \times 100. \quad (16)$$

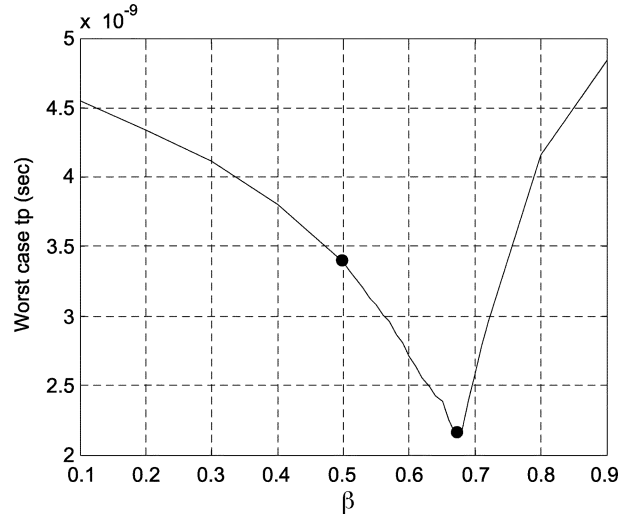


Fig. 5. Simulation results for worst-case propagation delay of the unidirectional bus, shown in Fig. 3, implemented in a METAL4 layer of a 0.18- μm CMOS technology.

Several simulations were performed on ELDO (a Mentor Graphics circuit simulation tool) to support the theory introduced in this paper. The simulation results in all the cases showed that the optimum worst-case propagation delay and the optimum area of the induced noise pulse occurred at a positioning exactly equal to the analytically derived β_{opt} . For example, the three-line 4500- μm -long unidirectional bus, shown in Fig. 3 was implemented in the Metal4 layer of a 0.18- μm TSMC CMOS technology. The repeaters were simple balanced inverters with an output resistance such that $\eta_r = 0.4$. The inverter's output resistance was calculated using the transistors' output resistance in the saturation mode. By substituting in (12), $\beta_{opt} = 0.68$. The lines were simulated while varying the interleaved repeater position, β . The worst-case propagation delay over the different switching conditions, on line 1 was recorded and plotted in Fig. 5. The simulation results show a minimum worst-case delay at the calculated β_{opt} . The results also show that at the commonly used $\beta = 0.5$, the delay is 79% higher than the minimum delay at β_{opt} . Note that this percentage improvement in delay is not general, but varies with the repeater and line characteristics as shown by (16).

B. Sensitivity to Interconnect Segment Length Variation

In the previous section, the segment length was assumed fixed when obtaining the optimum interleaved repeater position. In most literature, this segment length is assumed to be equal to the optimal segment length for minimum propagation delay, l_{opt} . In state-of-the-art VLSI designs, many predesigned and optimized subcircuits are reused. These design blocks have limited preallocated space for external routing which are usually just enough for interconnects without any repeaters. Thus, repeater insertion for external routing interconnects is usually limited to outside the borders of the subcircuit layouts [14]. Moreover, stringent limitations are put on maximum sizing and the number of repeaters, especially in buses, to reduce power supply collapse caused by a simultaneously switching bank of repeaters [3]. With such limitation on the number of repeaters and their positions, and as devices are continually scaled in modern technologies, the segment length between repeaters highly exceeds the optimal segment length for minimum propagation delay, l_{opt} , derived in [16]–[19]. So, as practical designs do not use the optimum segment length for minimum propagation delay, any bus scheme should not only be evaluated for its optimum propagation delay but also for the sensitivity of the propagation delay to segment length variation. In this section, the

performance sensitivity to length variations for buses with interleaved repeaters is analyzed.

The sensitivity of the propagation delay of an interconnect segment to its length is defined as

$$S_t(\beta, l) = \frac{\partial t_p(\beta, l)}{\partial l}. \quad (17)$$

In order to find the propagation delay sensitivity for the three switching cases discussed in II-A, (17) is applied to (8) to give

case 1 :

$$S_{t11}(\beta, l) = S_{to} + S_{tc}(1 + \eta_r)$$

case 2 :

$$S_{t20}(\beta, l) = S_{to} + 2S_{tc}(\beta + \eta_r)\beta$$

case 3 :

$$S_{t02}(\beta, l) = S_{to} + 2S_{tc}(1 + \beta + \eta_r)(1 - \beta) \quad (18)$$

where

$$S_{to} = 2.3 \times (rC_{inv} + R_{inv}c_g + rc_g l) \quad (19)$$

$$S_{tc} = 2.3 \times rc_c l. \quad (20)$$

The worst-case the sensitivity of the propagation delay of an interconnect segment to its length will thus be

$$S_t(\beta, l) = \max(S_{t11}(\beta, l), S_{t20}(\beta, l), S_{t02}(\beta, l)). \quad (21)$$

Substituting $\beta = 0.5$ and $\beta = \beta_{opt}$ in (21) yields

$$S_t(0.5, l) = S_{to} + S_{tc}(1.5 + \eta_r) \quad (22)$$

$$S_t(\beta_{opt}, l) = S_{to} + S_{tc}(2\beta_{opt}^2 + 2\beta_{opt}\eta_r). \quad (23)$$

However,

$$\frac{1}{2} < \beta_{opt} < \frac{1}{\sqrt{2}}. \quad (24)$$

This leads to

$$S_t(\beta_{opt}, l) < S_{to} + S_{tc}(1 + \sqrt{2}\eta_r). \quad (25)$$

In most current technologies $\eta_r < 1$, causing the sensitivity of an interconnect line with optimum repeater positioning provides less sensitivity to segment length variations to be less than that of an interconnect line with midway repeater positioning. The lower sensitivity to length variations proves to be highly advantageous in current VLSI designs as segment lengths increase beyond the optimum segment length, l_{opt} due to the uncertainty in repeater placement.

C. Area of the Noise Pulse on the Victim Line

In order to quantify the noise pulse on bus lines, consider the three adjacent bus lines in Fig. 3. Assume that line 1, the victim line, is quiet (has no switching activity), while the aggressor lines, lines 2 and 3, are switching similarly. Then, the area of the noise pulse induced on the victim line [15] is

$$A = \int_{-\infty}^{\infty} v_1(t).dt = V_m \sum_k C_{cTk} R_k \quad (26)$$

where $v_1(t)$ is the instantaneous voltage induced on the victim line and V_m is the steady-state voltage of the segment on the aggressor line with the rising activity. C_{cTk} is the total coupling capacitance (from both sides) downstream of node k on the victim line and, R_k is the

TABLE II
SWITCHING ACTIVITY COEFFICIENTS FOR DIFFERENT SWITCHING CONDITIONS OF SEGMENT 2

| Switching Case | α_{2l} | α_{3l} |
|--|---------------|---------------|
| 1. When segment 2 has a rising activity | 1 | -1 |
| 2. When segment 2 has a falling activity | -1 | 1 |

resistance of section k on the victim line. Applying the integral form of the summation in (26) to the victim line in Fig. 3, we obtain

$$A = V_m \int_0^{l'} (R_{inv} + rx).(\alpha_{12}.c_c)dx + V_m \int_{l'}^l (R_{inv} + rx).(\alpha_{13}.c_c)dx. \quad (27)$$

This integration evaluates to

$$A = V_m \left\{ \frac{rc_c}{2} [\alpha_{21}l'^2 + \alpha_{31}(l^2 - l'^2)] + R_{inv}c_c [\alpha_{21}l' + \alpha_{31}(l - l')] \right\} \quad (28)$$

$$A = V_{m_p}.t_{pc} \left\{ [\alpha_{21}\beta^2 + \alpha_{31}(1 - \beta^2)] + 2\eta_r [\alpha_{21}\beta + \alpha_{31}(1 - \beta)] \right\} \quad (29)$$

where t_{pc} , β , and η_r are as defined in (5)–(7), respectively. Each of the cases shown in Table II, will have an area of its noise pulse given by

case 1 :

$$A_1 = V_m t_{pc} \left\{ (2\beta^2 - 1) + 2\eta_r(2\beta - 1) \right\}$$

case 2 :

$$A_2 = -A_1. \quad (30)$$

In order to get a noise pulse with a zero average voltage, we require a certain optimal relative position ratio β'_{opt} that will make $A_1 = -A_2 = 0$. Hence, equating (30) to zero yields

$$1 + 2\eta_r = 2\beta'^2_{opt} + 4\eta_r\beta'_{opt}. \quad (31)$$

This result is exactly the same as (11) and, hence, the optimal relative position ratio, β'_{opt} , that gives a zero total area of the noise pulse of the victim line, is the same as the optimal relative position ratio, β_{opt} , that minimizes the propagation delay

$$\beta'_{opt} = \beta_{opt} = 0.5 \times \left[\sqrt{(2\eta_r + 1)^2 + 1} - 2\eta_r \right]. \quad (32)$$

Therefore, by positioning the interleaved repeaters at a relative position of $\beta_{opt}l$, both the propagation delay and the crosstalk induced on the line will be minimized. Since the area of the noise pulse is zero at optimal interleaved repeater positioning, the aggressor line acts as a virtual ground line.

If the repeaters on a line are positioned exactly midway between any two repeaters on the adjacent line, i.e. $\beta = 0.5$, this will lead to a nonzero noise pulse area, which is evident by substituting $\beta = 0.5$ in (30)

$$|A|_{mid} = 0.5 \times V_m t_{pc} > A_{opt} = 0. \quad (33)$$

The area of the noise pulse induced on line 1 in Fig. 3, with line 1 inactive, was also simulated and plotted in Fig. 6. The area of the noise pulse diminished to zero at β_{opt} . It should also be noted that the average area of the noise pulse at the commonly used $\beta = 0.5$, was significantly larger than zero as suggested by (33).

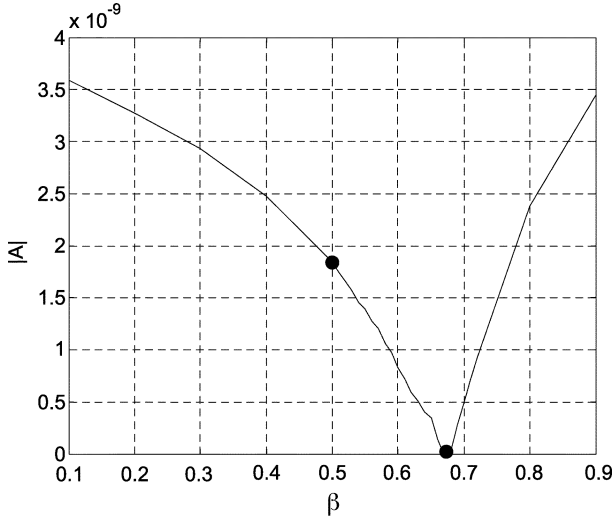


Fig. 6. Simulation results showing the area of the noise pulse for the unidirectional bus, shown in Fig. 3, implemented in a METAL4 layer of a $0.18 \mu\text{m}$ CMOS technology.

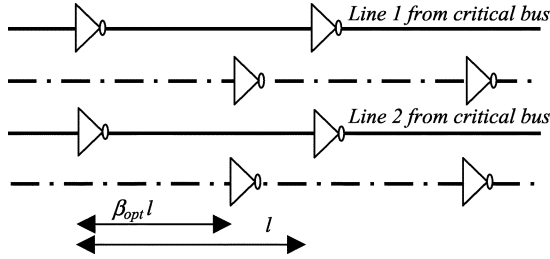


Fig. 7. Two buses combined together such that their lines alternate. Interleaved repeaters are inserted in both but optimally positioned on the adjacent lines of the critical bus to improve their performance.

D. Practicality of the Optimal Interleaved Repeater Positioning Scheme

In the previous sections, it was shown that inserting the interleaved repeaters at a relative position given by $\beta_{\text{opt}} l$ gives the optimum performance. This repeater positioning, however, cannot be practically applied to unidirectional buses. The reason can be explained based on the unidirectional two-line bus illustrated in Fig. 3. Even though placing inverter c at a relative distance $\beta_{\text{opt}} l$ from inverter a optimizes the performance on line 1, the relative position of inverter b with respect to inverter c is $(1 - \beta_{\text{opt}}) \times l \neq \beta_{\text{opt}} l$. Hence, although the performance of line 1 is optimized, the performance of line 2 will be degraded compared to midway positioning. Thus, the only solution to balance the performance of both lines is to place the interleaved repeaters midway between each two repeaters on the adjacent line, i.e., $\beta = 0.5$, as shown in Fig. 2. This is currently implemented in unidirectional buses.

It is also worth stating that optimally positioned interleaved repeaters in unidirectional buses can improve the system performance if two neighboring buses exist, such that the delay of only one of them is critical. In that case, the two buses can be combined, such that their lines alternate, and the optimally positioned interleaved repeaters are placed, such that the performance of the lines of the critical bus is improved. This case is illustrated in Fig. 7.

Although the optimal positioning of interleaved repeaters is not generally practical for unidirectional buses, it can be efficiently implemented in bidirectional buses, as shown in Fig. 8, to improve their delay and noise performance. This is discussed in the following section and compared to other commonly used bidirectional buses.

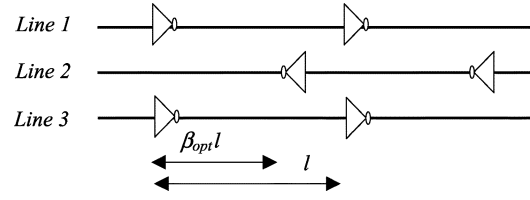


Fig. 8. Bidirectional bus with optimally positioned interleaved repeaters.

III. BIDIRECTIONAL BUSES WITH OPTIMALLY INTERLEAVED REPEATERS

Optimal positioning of interleaved repeaters was shown in the previous section to be generally impractical for unidirectional buses, as optimal repeater positioning on a line leads to nonoptimal repeater positioning on its adjacent lines. However, if optimal repeater positioning is applied to bidirectional buses, as shown in Fig. 8, then the distance between any repeater and the adjacent interleaved repeater in the signal propagation direction will always be the optimum interleaved repeater spacing $\beta_{\text{opt}} l$. The previous analysis can be extended to derive the optimal positioning of interleaved repeaters in bidirectional buses, which yields the same previously derived optimum position (12).

This section provides simulation results showing the effect of optimum positioning of interleaved repeaters in *bidirectional* buses on the propagation delay, the noise pulse area and peak, and the sensitivity to segment length variation. Finally, the throughput per unit area of the proposed bidirectional bus with optimally positioned interleaved repeaters is compared to that of conventional bidirectional buses.

A. Optimum Interleaved Repeater Position for Minimal Propagation Delay

Several simulations were performed on ELDO to record the variation of the worst-case propagation delay as the repeater positioning ratio β is changed. The simulation results in all the cases showed that the optimum worst-case propagation delay and the optimum area of the induced noise pulse occurred at a positioning exactly equal to the analytically derived β_{opt} . For example, a three-line $4500\text{-}\mu\text{m}$ -long bidirectional bus, shown in Fig. 8, was implemented in the Metal4 layer of a $0.18\text{-}\mu\text{m}$ TSMC CMOS technology. The repeaters were simple, balanced inverters with an output resistance such that $\eta_r = 0.4$. The inverter's output resistance was calculated using the transistors' output resistance in the saturation mode. By substituting in (12), $\beta_{\text{opt}} = 0.68$. The lines were simulated while varying the interleaved repeater position β . The worst-case propagation delay over the different switching conditions, on the middle line was recorded and plotted in Fig. 5. The simulation results show a minimum worst-case delay at the calculated β_{opt} . The results also show that at the commonly used $\beta = 0.5$, the delay is 36% higher than the minimum delay at β_{opt} . Note that this percentage improvement in delay is not general but varies with the repeater and line characteristics, as shown by (16).

Note that the percentage improvement in the propagation delay, due to optimally positioning the interleaved repeaters as compared to midway positioning, decreased from 79% for unidirectional buses, as shown in Fig. 5, to 36% for bidirectional buses as shown in Fig. 9. The reason behind the reduction in the percentage delay improvement is that the propagation delay of the unidirectional bus, shown in Fig. 3, is generally higher than that of the bidirectional bus, shown in Fig. 8, for the same segment lengths and repeater sizes, because oppositely switching lines will continuously switch oppositely throughout most of the unidirectional bus length. However, adjacent lines in bidirectional buses switch oppositely *only* during a certain region of the bus when the oppositely traveling signals cross each other. The difference in delays between unidirectional and bidirectional buses depend on the

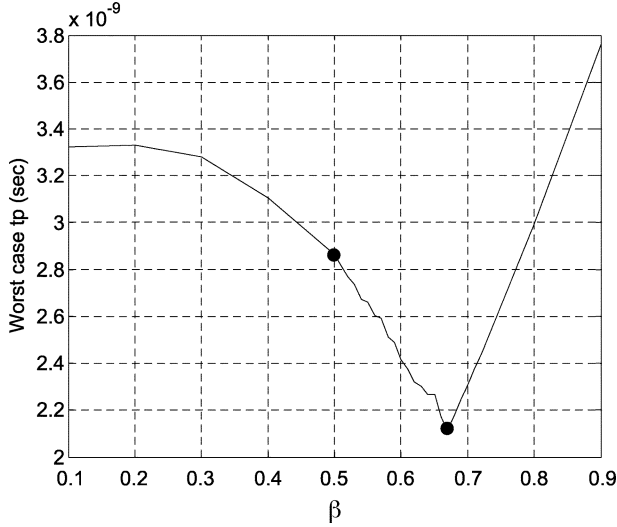


Fig. 9. Simulation results for worst-case propagation delay of the bidirectional bus, shown in Fig. 8, implemented in a METAL4 layer of a 0.18- μm CMOS technology.

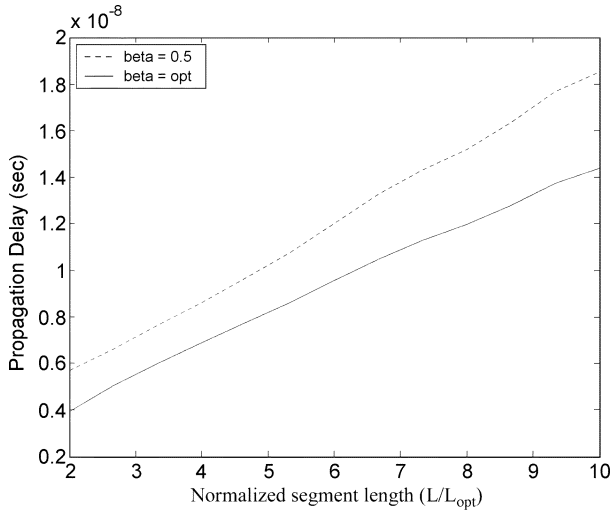


Fig. 10. Simulation results for worst-case propagation delay of the bidirectional bus, shown in Fig. 8, implemented in a METAL4 layer of a 0.18- μm CMOS technology. The total interconnect length is kept constant to $100 l_{\text{opt}}$ while the segment length l is varied. The segment length is normalized here to the optimum segment length, $l_{\text{opt}} = 450 \mu\text{m}$.

ratio between the rise/fall times of the signals on the adjacent lines when they cross each other and the total propagation delay. Also, note that the optimum (minimum) propagation delay for both unidirectional and bidirectional buses, as shown in Figs. 5 and 9, are the same for the same segment lengths and repeater sizes. This is expected because the minimum propagation delay, when $\beta = \beta_{\text{opt}}$, is equivalent to the propagation delay when one line is switching *while its adjacent lines are static* (10), and in this specific situation both unidirectional and bidirectional buses will behave similarly.

B. Sensitivity to Interconnect Segment Length Variation

The same three-line bidirectional bus implemented in the Metal4 layer of a 0.18- μm TSMC CMOS technology, and shown in Fig. 8, was simulated again while keeping the total interconnect length and repeater output resistance constant, but varying the segment length.

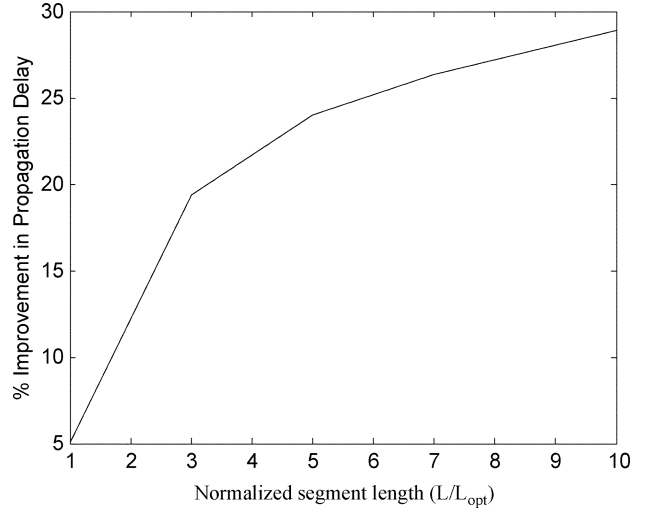


Fig. 11. Simulation results for the relative penalty in a segment's propagation delay, when using midway repeater positioning rather than optimum repeater. The bidirectional bus, shown in Fig. 8 was implemented in a METAL4 layer of a 0.18- μm CMOS technology. The segment length is normalized here to the optimum segment length, l_{opt} .

Thus, the number of segments also varied. The total worst-case propagation delay of the complete interconnect was recorded for the two cases of optimum and midway repeater positioning. The simulation results, shown in Fig. 10, show that the variation of the worst-case propagation delay in the case of optimum repeater positioning is less severe (lower slope) than the case of midway repeater positioning.

It is also important to note that the relative penalty in propagation delay, when using midway repeater positioning rather than optimum repeater positioning saturates as the segment length increases. For a very large segment length

$$t_{\text{po}} \rightarrow 2.3 \times \frac{rc_g l^2}{2} \quad (34)$$

$$t_{\text{pc}} \rightarrow 2.3 \times \frac{rc_c l^2}{2} \quad (35)$$

$$\eta_r = \frac{R_{\text{inv}}}{rl} \ll 1. \quad (36)$$

By substituting from (34)–(36) in (16), the relative penalty limit in propagation delay due to using midway repeater positioning turns out to be a technology-dependent ratio, as shown in (37). This ratio is always increasing with technology scaling, as shown in Fig. 1

$$\left. \frac{\Delta t_p}{t_{p,\text{opt}}} \right|_{\text{max}} = \frac{0.5 \times 2.3 \times \frac{rc_c l^2}{2}}{2.3 \times \frac{r(c_g + c_c)l^2}{2}} = \frac{c_c}{c_g + c_c}. \quad (37)$$

The saturation of the relative penalty in propagation delay was confirmed from the simulation results as shown in Fig. 11.

C. Area of the Noise Pulse on the Victim Line

The area of the noise pulse induced on the middle line of the bidirectional bus in Fig. 8, with the middle line inactive, was also simulated and plotted in Fig. 6. The area of the noise pulse diminished to zero at β_{opt} . It should also be noted that the average area of the noise pulse at the commonly used $\beta = 0.5$, was significantly larger than zero, as suggested by (33). Note also that the values of the noise pulse area of unidirectional buses in Fig. 6 are similar to those for bidirectional buses in Fig. 12, which is expected because the noise pulse is measured on a quiet line in both buses, shown in Figs. 3 and 8, while its two adjacent

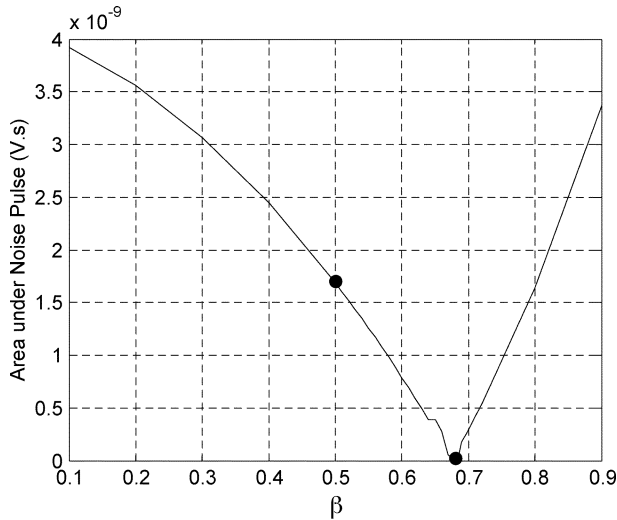


Fig. 12. Simulation results showing the area of the noise pulse for of the bidirectional bus, shown in Fig. 8.

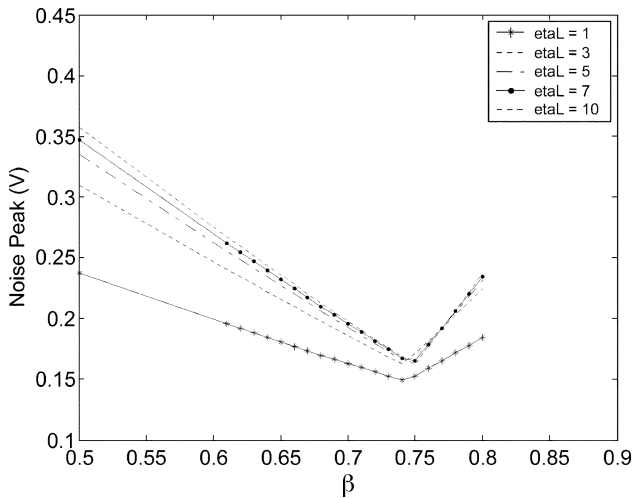


Fig. 13. Simulation results showing the variation of the peak of the noise pulse, as the interleaved repeater position and the segment length were varied. These results are for the bidirectional bus, shown in Fig. 8 implemented in a METAL4 layer of a 0.18 μm CMOS technology.

lines are similarly switching. Thus, the unidirectional and bidirectional buses will behave similarly under this setup and yield similar results.

D. Amplitude of the Noise Pulse on the Victim Line

In order to record the amplitude of a noise pulse on bus lines, the same three-line bidirectional bus in Fig. 8 is considered. The middle line, the victim line, will also be assumed to be quiet (has no switching activity), while the aggressor lines, lines 1 and 3, are similarly switching. Some preliminary analysis and extensive simulations were done to find the interleaved repeater positioning for minimum noise peak. The simulation results are shown in Fig. 13. The results show that the interleaved repeater-positioning ratio (β) for minimum noise peak is higher than that for minimum propagation delay. Hence, the noise peak at the optimum repeater position for optimum delay will always be lower than that for midway repeater position, as shown in Fig. 14, leading to a lower chance of logic errors.

The sensitivity of the amplitude of the noise pulse to segment length appears to decrease as the segment length increases, as shown in Fig. 14. The noise pulse amplitude for a certain relative repeater

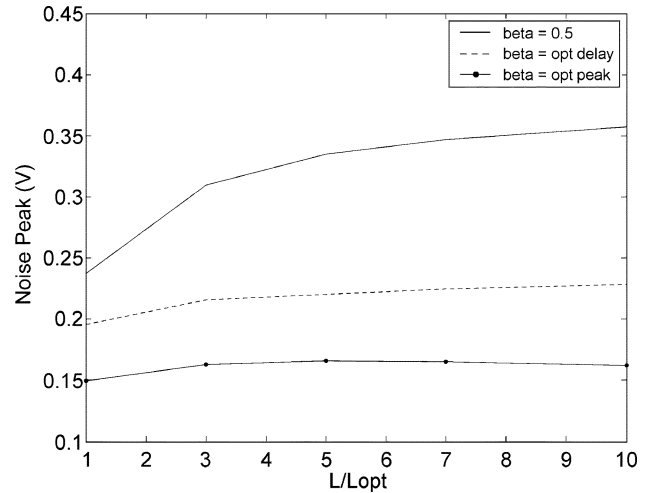


Fig. 14. Simulation results showing the sensitivity of the noise pulse amplitude to the segment length.

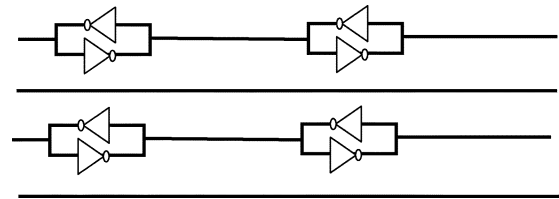


Fig. 15. Conventional shielded bidirectional bus (with static lines alternating with signal lines).

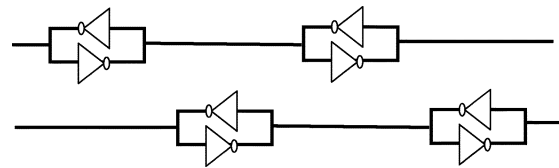


Fig. 16. Conventional bidirectional bus with midway positioned interleaved repeaters.

position saturates to a value that can be proven to depend only on the relative repeater positioning ratio β and the ratio of the lateral to vertical capacitance c_c/c_g . These results provide designers with the flexibility of increasing the interconnect segment length without worrying much about the noise pulse amplitude, as it will saturate to a value that can be controlled by the interconnect dimensions. It can also be observed from Fig. 14 that the amplitude of the noise pulse saturates at a shorter segment length for optimum repeater positioning β_{opt} , as compared to midway repeater positioning, $\beta = 0.5$. Thus, using optimum rather than midway repeater positioning not only provides a lower noise pulse amplitude limit, but also provides variation of noise pulse amplitude in a smaller range of segment lengths.

E. Comparing the Bidirectional Bus With Optimally Positioned Interleaved Repeater to Conventional Bidirectional Buses

In current integrated circuits, there are two main implementations of on-chip bidirectional buses shown in Figs. 15 and 16. The first, shown in Fig. 15, is a shielded half-duplex bidirectional bus, which consists of a set of lines with bidirectional buffers and static lines (ground or power lines) in between. Fig. 16 shows an unshielded half-duplex bidirectional bus with midway interleaved repeaters that consists of a set of lines with interleaved bidirectional repeaters inserted midway between any two repeaters on the adjacent line, $\beta = 0.5$. In each of these two

implementations, the data may flow in both directions on each of the signal lines but not simultaneously.

The bidirectional bus with optimally positioned interleaved repeaters is a set of unidirectional lines such that lines with opposite data flow alternate. Each line has interleaved repeaters inserted at the optimal relative position $\beta_{opt}l$, as illustrated in Fig. 17.

Another possible bidirectional bus implementation is the unshielded full-duplex bidirectional bus with midway interleaved repeaters, as shown in Fig. 18. The bidirectional bus shown in Fig. 18 consists of a set of unidirectional lines with midway interleaved repeaters, $\beta = 0.5$, such that lines with opposite data flow alternate. This implementation is added in the following comparison for the sake of completeness.

In order to fairly compare between the commonly used bidirectional bus implementations and the bidirectional bus with optimally positioned interleaved repeaters, a figure of merit M defined as the bit rate per bus area will be used. Also, the length per section, the wire pitch s , and the used inverters are kept the same, and hence η_r , c_c , and t_{pc} will remain the same.

$$M = \frac{B}{n \cdot (w + s) \cdot L} \quad (38)$$

where B is the bit rate of the bus, n is the number of bus lines, w is the physical width of the line, s is the signal line pitch and L is the length of the bus.

The bit rate is proportional to the reciprocal of the propagation delay, i.e.,

$$B = \frac{\gamma}{t_p} n_s \quad (39)$$

where γ is a proportionality constant and n_s is the number of signaling bus lines. (38) can be rewritten as

$$M = \frac{\gamma \cdot n_s}{t_p \cdot n \cdot (w + s) \cdot L} \quad (40)$$

The figure of merit for the bidirectional bus with optimally positioned interleaved repeaters ($n_s = n$), shown in Fig. 17, will be

$$M_0 = \frac{\gamma \cdot n}{t_{p,0} \cdot n \cdot (w + s) \cdot L} = \frac{\gamma}{t_{p,0} \cdot (w + s) \cdot L} \quad (41)$$

where $t_{p,0}$ is the optimum propagation delay of each line given by

$$t_{p,0} = t_{p,0,0} + 2t_{pc}\{1 + 2\eta_r\}. \quad (42)$$

Note that this optimum propagation delay is the same as that defined in (14) but as each line is sandwiched between two lines, the coupling capacitance is doubled.

In the bidirectional bus implementation, shown in Fig. 15, the figure of merit will be

$$M_1 = \frac{\frac{\gamma \cdot n}{2}}{t_{p,1} \cdot n \cdot (w + s) \cdot L} = \frac{\gamma}{2t_{p,1} \cdot (w + s) \cdot L} \quad (43)$$

where $t_{p,1}$ is the propagation delay of each line given by

$$t_{p,1} = t_{p,0,1} + 2t_{pc}\{1 + 2\eta_r\}. \quad (44)$$

As the static line is not used for data signaling, only half of the bus lines are effectively sending data and hence $n_s = n/2$.

In the bidirectional bus implementation, shown in Fig. 16, the figure of merit will be

$$M_2 = \frac{\gamma \cdot n}{t_{p,2} \cdot n \cdot (w + s) \cdot L} = \frac{\gamma}{t_{p,2} \cdot (w + s) \cdot L} \quad (45)$$

where $t_{p,2}$ is the propagation delay of each line given by

$$t_{p,2} = t_{p,0,2} + 2t_{pc}\{1.5 + 2\eta_r\}. \quad (46)$$

In addition, note that bidirectional repeaters [20] or boosters [21] implemented in the commonly used bidirectional buses have five to

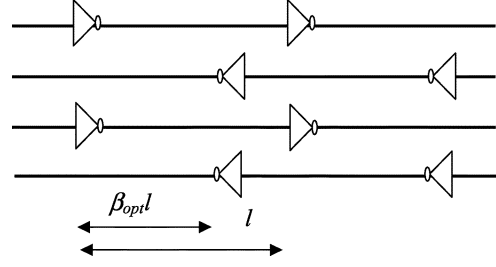


Fig. 17. Bidirectional bus with optimally positioned interleaved repeaters.

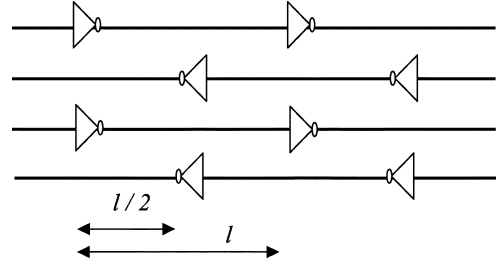


Fig. 18. Bidirectional bus with midway positioned interleaved repeaters.

seven times the number of transistors in unidirectional repeaters. This implies that bidirectional repeaters and boosters have higher parasitics and, thus, $t_{p,0,1} = t_{p,0,2} > t_{p,0,0}$. So, by comparing (41) and (43)

$$\frac{M_0}{M_1} = \frac{2t_{p,1}}{t_{p,0}} = \frac{2 \cdot [t_{p,0,1} + 2t_{pc}\{1 + 2\eta_r\}]}{t_{p,0,0} + 2t_{pc}\{1 + 2\eta_r\}} > 2. \quad (47)$$

M_0 is at least twice as M_1 . This indicates that the bidirectional bus with optimally positioned interleaved repeaters provides higher bit-rate per unit bus area. Moreover, the two buses have comparable noise performance since the adjacent lines to any signal line in the bidirectional bus with optimally positioned interleaved repeaters appear as virtual static lines and in the bus implementation shown in Fig. 15 each signal line is sandwiched between physically static lines.

By comparing (41) and (45), we get

$$\frac{M_0}{M_2} = \frac{t_{p,2}}{t_{p,0}} = \frac{[t_{p,0,2} + 2t_{pc}\{1.5 + 2\eta_r\}]}{t_{p,0,0} + 2t_{pc}\{1 + 2\eta_r\}} > 1. \quad (48)$$

M_0 will be higher than M_2 due to the optimum repeater positioning and the simpler unidirectional buffers used in the bidirectional bus with optimally positioned interleaved repeaters. Thus, the bidirectional bus with optimally positioned interleaved repeaters has a higher bit-rate per unit bus area than that of the bus implementation shown in Fig. 16. The amount of improvement will depend on the line and repeater parameters. Moreover, the noise performance of the bidirectional bus with optimally positioned interleaved repeaters is much better, since the area of the noise pulse induced on any line is zero as was discussed in the previous section.

For the full-duplex bidirectional bus with midway interleaved repeaters, shown in Fig. 18, the figure of merit will be

$$M_3 = \frac{\gamma \cdot n}{t_{p,3} \cdot n \cdot (w + s) \cdot L} = \frac{\gamma}{t_{p,3} \cdot (w + s) \cdot L} \quad (49)$$

where $t_{p,3}$ is the propagation delay of each line given by

$$t_{p,3} = t_{p,0,3} + 2t_{pc}\{1.5 + 2\eta_r\}. \quad (50)$$

By comparing (41) and (49), we get

$$\frac{M_0}{M_3} = \frac{t_{p,3}}{t_{p,0}} = \frac{[t_{p,0,3} + 2t_{pc}\{1.5 + 2\eta_r\}]}{t_{p,0,0} + 2t_{pc}\{1 + 2\eta_r\}} > 1. \quad (51)$$

M_0 will be higher than M_3 due to the optimum repeater positioning. Thus, the proposed bidirectional bus with optimally positioned interleaved repeaters has a higher bit-rate per unit bus area than that of the bus implementation shown in Fig. 18. The amount of improvement will depend on the line and repeater parameters. Moreover, the noise performance of the bidirectional bus with optimally positioned interleaved repeaters is much better, since the area of the noise pulse induced on any line is zero as was discussed in the previous section.

IV. CONCLUSION

Buses are one of the main bottlenecks in improving the performance of state-of-the-art integrated circuits. Several aspects of recent DSM technologies limit the maximum bit rate that can be sent on the bus as well as degrade the signal integrity. In this paper, a new positioning scheme for the interleaved repeaters was introduced. The new positioning was shown to provide better propagation delay and noise performance than the commonly used midway positioning scheme. Moreover, the presented optimum repeater positioning was proven to offer lower noise pulse amplitude as well as lower sensitivity of propagation delay and noise pulse amplitude to segment length variation, compared to commonly used midway repeater positioning.

Optimal interleaved repeater insertion was shown to be impractical in implementing unidirectional buses. However, bidirectional buses with optimally positioned interleaved repeaters showed superior performance in bit rate per unit area. The amount of improvement depends mainly on the characteristics of the bus lines and the repeater used and can exceed 50%, compared to common bidirectional buses. Moreover, with this optimum repeater placement, the area of the noise pulse of victim lines is zero indicating that aggressor bus lines are virtually static.

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Intrabus Crosstalk Estimation Using Word-Level Statistics

Suvodeep Gupta and Srinivas Katkoori

Abstract—We propose two word-level statistical techniques to estimate the probability of crosstalk events on the signal lines of a system bus. Given the word-level statistical parameters, namely mean, standard deviation, and lag-one temporal correlation coefficient, we analytically estimate the bit-level crosstalk probability. To linearize the complexity and efficiently scale the estimation technique for large bus-widths, we modify the first technique by using a circular right shift procedure that maps disjoint values in a distribution to continuous values in a modified distribution. Experimental results for data streams from different data environments, compared against detailed HSPICE simulations, are presented. The statistical estimators yield average errors less than 7% and 12%, respectively, for bus-widths ranging from 8 to 32 bits. Compared to HSPICE, the execution times are reduced by factors of over $10 \times$ for the first technique and over two orders of magnitude for the second technique. The statistical approaches are shown to be compatible with existing bus reordering techniques.

Index Terms—Crosstalk, high-level estimation, statistics.

I. INTRODUCTION AND RELATED WORK

Coupled noise between signal lines is an increasingly important problem for high-speed digital circuits. In deep submicron (DSM) technologies, the coupling capacitance between wires in the vicinity of one another is significant compared to their individual wire-to-substrate capacitances. This problem is particularly serious for on-chip

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