

Analysis of Coupling Noise and it's Scalability in Dynamic Circuits

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Abstract: The usage of noise sensitive dynamic circuits has become commonplace due to speed and area requirements, making the noise issue even more prominent. This paper focuses on the trends of coupling and its effects on dynamic circuits. The paper presents closed form analytical solutions for noise as well as noise tolerance metrics for dynamic circuits. These solutions are within 5% of dynamic simulations. It is shown that not all scaling trends are negative for noise, and that the scaling down of supply voltage and increasing frequency help improve certain aspects of the noise immunity of dynamic circuit. Most of the work treated the noise immunity and the noise content separately. This paper introduces an analysis of noise scalability by looking at the noise immunity and the noise content simultaneously.

1. Introduction

With the continued scaling in modern deep submicron CMOS processes, noise has become an equally important metric to area, timing and power dissipation [1]-[4],[10],[11]. Performance requirements are driving designs in the direction of using noise-sensitive dynamic circuits, making the analysis of noise effects more important. Dynamic logic is gaining popularity for its attractive features of reduced transistor count with a reduced capacitive load resulting in lower area and increased speed for CMOS circuits [1]. In static circuits momentary deviation of logic levels can be restored automatically, since at steady state the nodes are always connected either to ground or V_{dd} . However, this restoration is not possible in dynamic circuits due to the possibility of floating nodes. Fig.1 illustrates the susceptibility of dynamic logic by a simple example of two inverters. Because of the dramatic reduction in the supply and threshold voltages with the continuous scaling of CMOS technologies, the noise margins have been significantly decreased. In static logic the N and the P blocks can be balanced to obtain the highest possible noise margins. But in the case for dynamic logic, the noise margins can be as low as V_{tr} . Lower threshold voltages also result in increased leakage noise.

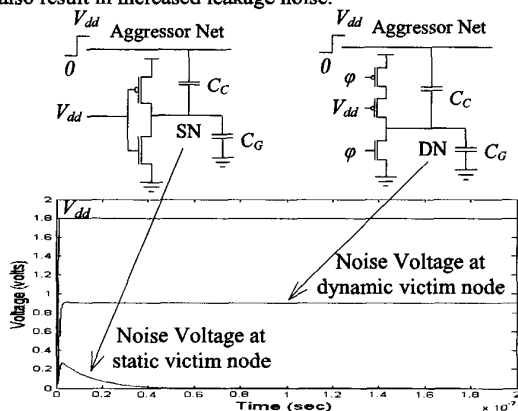


Fig.1. Effect of Noise on Static and Dynamic Nodes

Among the various sources of noise in current deep submicron CMOS technologies the noise due to capacitive and inductive coupling has become dominant. Coupling noise imposes two serious side effects on digital integrated circuits. Coupling can cause the

effective line capacitance and inductance to increase or decrease in the presence of simultaneously switching coupled lines, increasing or decreasing the signal delay. Second, it can cause functional failures by charging or discharging the capacitor responsible for holding the logic level at a dynamic node. To analyze the effects of coupling it is not the absolute value of the coupling capacitance that has to be considered. The two factors, that affect circuit performance, are (i) the ratio between the coupling capacitance to the total capacitance, and (ii) the switching or coupling factor. In current CMOS technologies the total capacitance is estimated as the sum of four components: (i) line-to-ground capacitance, (ii) coupling or lateral capacitance (between two nets on the same layers), (iii) parallel or crossover capacitance (due to overlap area of two nets on different layers), and (iv) fringing capacitance (formed between the edge of one conductor and the surface of another conductor on different layers) [6]-[9]. The total capacitance of a certain conductor (for example conductor-1 in Fig.2) in a multi-layer representation is given by

$$C_{total} = C_{gnd} + C_l + C_p + C_f \quad (1)$$

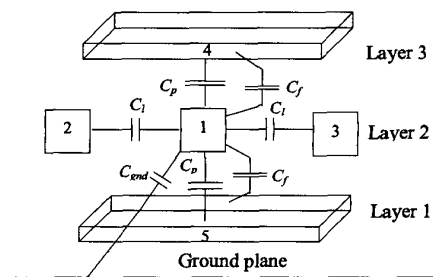


Fig.2. Capacitances of a conductor in a multi-layer representation

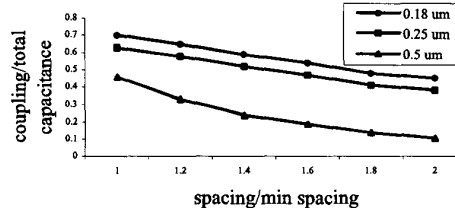


Fig.3. Coupling capacitance compared to total capacitance with technology scaling [10],[12]

Due the recent trends of technology scaling, the ratio between the coupling or lateral capacitance to the total capacitance is increasing (see Fig.3 [10], [12]). The coupling capacitance (C_l) is becoming stronger due to the decrease of spacing between conducting lines, the increase of interconnect length and aspect ratio, and the longer overlap area among lines in the same layers [6]-[12]. This is particularly true in the upper metal layers, where power and clock distribution networks, and global signal lines run across the whole chip area. Bus-dominant design worsens the effects of coupling, since it results in longer parallel wires. This growing coupling can affect circuit operation severely depending on the switching or coupling factor. Since most lines have two parallel

neighboring lines on two sides, the total coupling factor for a line is in the range of zero to four [13]. In the worst case the coupling factor is 4.

Most of the previous work treated the noise immunity and the noise content separately, and emphasized the fact that noise immunity of CMOS digital integrated circuits degrades with the scaling of technology. However, it is important to note that the noise content in dynamic circuit decreases with the scaling down of supply voltage. Moreover, with the increase of clock frequency, the injected noise in a dynamic circuit will have less time to disrupt (charge or discharge) the capacitor holding the logic level at the dynamic node. This time is typically half a clock cycle for symmetric clocks. As a result dynamic circuits may tolerate higher noise at higher frequencies. Therefore, while the overall trends of modern CMOS technology make CMOS digital circuits more susceptible to noise, decreasing supply voltage and increasing frequency actually have positive effects on the noise tolerance of dynamic circuits. Consequently, a more realistic and positive analysis of noise scalability in dynamic circuit is imperative. This paper focuses on the coupling noise issues in dynamic circuits. The rest of the paper is organized as follows. Section 2 presents a simple and accurate formula to calculate the induced noise voltage on a dynamic node due to coupling. Section 3 presents closed form analytical solutions for noise tolerance metrics for dynamic circuits. Section 4 introduces a positive analysis of noise in dynamic circuit and presents the idea of noise scalability with technology scaling. Section 5 concludes the paper.

2. Noise voltage at dynamic node due to coupling

As coupling becomes stronger, the noise content injected into a dynamic circuit through coupling is increasing. The magnitude of the induced noise voltage on the dynamic victim node N (see Fig.4) due to switching of the aggressor net depends on the ratio of the total effective coupling capacitance (C_{CT}) to the total capacitance of the victim net ($C_{TOTAL} = C_{CT} + C_{GT}$).

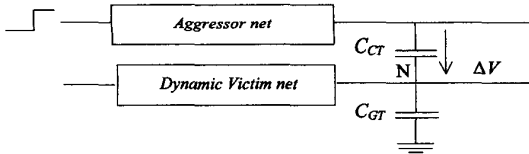


Fig.4. Coupling of a dynamic net

Here C_{GT} includes all the components of capacitance of the victim net except the lateral or coupling capacitance. When the victim net is quiet and the aggressor net is switching from low to high, the magnitude of the induced noise voltage (ΔV) on the dynamic victim node can be given by simple voltage divider formula (2).

$$\Delta V = \frac{C_{CT} \cdot V_{dd}}{C_{CT} + C_{GT}} = \frac{C_{CT}}{C_{TOTAL}} \cdot V_{dd} \quad (2)$$

SPICE simulations (Table 1) of three pairs of coupled interconnect lines with increasing C_{CT}/C_{TOTAL} ratios give exactly the same results as equation (2). It is observed from (2) as well as from the simulations that for a certain V_{dd} the magnitude of the induced noise ΔV linearly increases with the C_{CT}/C_{TOTAL} ratio.

It is important to note that the self and mutual inductances won't affect the final magnitude of the injected noise voltage ΔV . Inductances will contribute some initial overshoots and oscillations, but the final value of ΔV depends purely on the ratio C_{CT}/C_{TOTAL} (see Fig.5). Also increasing frequency won't have any effect on the final

magnitude of the noise voltage ΔV . At higher frequency the final value of ΔV will be reached faster.

Table 1: Induced Noise Voltage on Dynamic Node

		C_{CT}/C_{TOTAL}								
		0.36			0.41			0.45		
V_{dd} (volts)		3	1.8	1.08	3	1.8	1.08	3	1.8	1.08
ΔV	Simulation	1.06	0.635	0.38	1.2	0.72	0.431	1.361	0.82	0.491
	Eqn. (2)	1.07	0.64	0.386	1.2	0.72	0.432	1.364	0.82	0.49

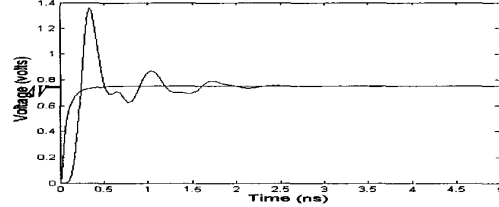


Fig.5. Effects of inductances on the noise level

3. Noise tolerance metrics for dynamic circuits

If the victim net of Fig.4 drives a dynamic circuit (see Fig. 6), the induced noise voltage ΔV will propagate through the dynamic circuit and affect the operation of the driven circuit depending on the magnitude and the direction of ΔV . Consider the case when V_{out} is precharged to V_{dd} . In the evaluation mode (with $\phi = "1"$ and $V_{in} = "0"$), if ΔV lowers the victim net voltage below "0", it will cause bootstrapping in the driven circuit.

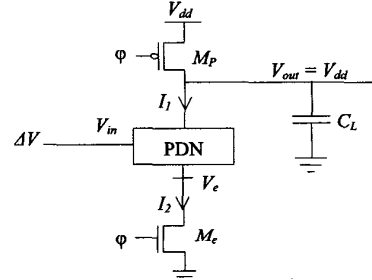


Fig. 6. Effect of ΔV on dynamic circuit operation

If ΔV raises the victim net voltage above V_{in} , the PDN network turns ON, and V_{out} starts to discharge. In this case, the PDN is assumed to be a single NMOS transistor such as in a NOR gate, which represents a worst-case noise effect. Using the α -power law model [14] for the devices, the discharge current can be given by

$$I = I_1 = I_2 \quad (3)$$

where,

$$I_1 = p_c (\Delta V - V_e - V_m)^\alpha \quad (4)$$

$$I_2 = \frac{p_c}{p_v} (\phi - V_m)^{\alpha/2} \cdot V_e \quad (5)$$

Here α is the velocity saturation constant; p_c and p_v are the constants that characterize the current drive capability of the transistor in the saturation and in the linear region, respectively. Here the clock signal $\phi = V_{dd}$. Iteratively solving (3), (4) and (5) we get the expression (6) for the discharge current as a function of ΔV .

$$I = p_c (\Delta V - V_e - V_m)^\alpha \quad (6)$$

$$\text{where } V_e = p_v \left[\frac{\Delta V - V_{e1} - V_m}{(V_{dd} - V_m)^{1/2}} \right]^\alpha \text{ and } V_{e1} = \frac{\Delta V - V_m}{1 + \frac{1}{p_v} (V_{dd} - V_m)^{1/2}}$$

In this iterative solution of V_e to calculate discharge current I , we

made an initial guess of $\alpha = I$, which is a good approximation for deep submicron circuits.

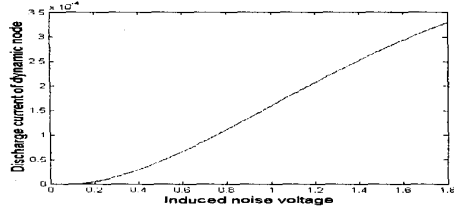


Fig. 7 Increase of discharge current I with noise voltage ΔV

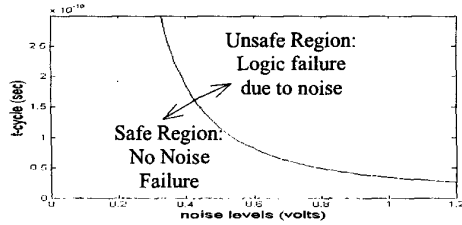


Fig. 8 Safe noise voltage level at a certain cycle time

It is clear from (6) that the discharge current I increase almost linearly with ΔV . Simulation results (see Fig. 7) for MOSIS TSMC 0.18 μ m technology also reveal the fact that higher noise voltage (ΔV) on the victim net results in faster discharge of the dynamic output node voltage of the driven circuit. Since the discharge current is constant at a certain level of ΔV over the time of interest (see Fig. 7), the change of the output voltage with time can be given by

$$V_{out}(t) = V_{dd} - \frac{I \cdot t}{C_L} \quad (7)$$

Here the magnitude of the output voltage change ($\frac{I \cdot t}{C_L}$) is directly

proportional to the discharge current (I), which is a function of ΔV . Therefore, with the increase of ΔV the output voltage falls further below the correct logic level (which is V_{dd} in this case). If $\frac{I \cdot t}{C_L}$

becomes equal to or greater than NM_H of the dynamic circuit, eventually a functional failure occurs. The magnitude of the output voltage change is time dependent. For a certain level of ΔV , the discharge current will remain for a shorter period of time with smaller clock cycle. To investigate when a circuit will fail for a certain noise level, consider that the circuit will fail at $V_{out}(t) = qV_{dd}$, where the multiplying factor q is in the range [0-1], which depends on the noise margins. For an ideal inverter, which has a

switching threshold of $\frac{V_{dd}}{2}$, the value of q is 0.5. Higher value of q

means lower noise margin or larger factor of safety. From (7) we get

$$t = \frac{V_{dd} - V_{out}(t)}{I} \cdot C_L \quad (8)$$

Therefore, the time for a dynamic circuit to fail can be given by

$$t_{failure} = \frac{(1-q) \cdot V_{dd} \cdot C_L}{I} \quad (9)$$

From (6) and (9) it can be inferred that with higher ΔV (higher I), the dynamic circuit will fail quickly, and with smaller cycle time the circuit can tolerate higher ΔV without functional failure. Therefore for a circuit to operate without any functional failure due to noise, the limit on the clock cycle time is (assuming a symmetric clock)

$$t_{cycle} < 2 \cdot t_{failure} \quad (10)$$

For a certain ΔV , the dynamic output voltage will be discharged below the noise margin and a logic error will occur when

$$t_{cycle} \geq 2 \cdot t_{failure} \quad (11)$$

By plotting $t_{cycle} = 2 \cdot t_{failure}$ as function of ΔV we can define an area of safe operation for the dynamic circuit (see Fig. 8 for TSMC 0.18 μ m technology). Here we consider $q = 0.7$. That is, noise margin $NM_H = 0.3V_{dd}$.

For reliable operation the operating point of the dynamic circuit must be lower than the ΔV - t_{cycle} curve in Fig. 8. For example, with $\Delta V = 0.6$ volts the circuit of Fig. 6 will have a functional failure with a clock cycle of 0.81ns or higher, and the corresponding time at which V_{out} falls below qV_{dd} (1.26 volts) is 0.405ns. Dynamic simulations (Table 2 and Fig. 9) give the same results with very low margin of error. From Fig. 9 it is observed that as the noise level increases from 0.6volts to 1.0volts, the functional failure time for the dynamic circuit decreases from 0.409ns to 0.172ns. The calculation error between the expression and the simulation is higher at lower noise level, but it is not that significant since at lower noise level there is less possibility of functional error. The proposed expressions are more accurate at higher ΔV , which is the region of most interest.

Table 2: Failure time at different noise voltage ($q = 0.7$)

		ΔV (volts)			
		0.4	0.6	0.8	1.0
Analytical value	$t_{failure}$	0.93ns	0.405ns	0.245ns	0.170ns
Simulation	$t_{failure}$	0.845ns	0.409ns	0.249ns	0.172ns
% Error		10	1	1.6	1.2

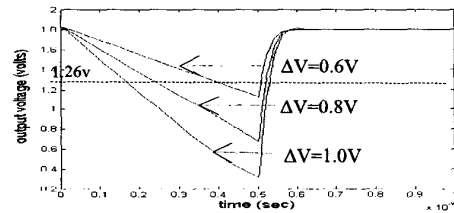


Fig. 9 Functional failure at different levels of noise

Dynamic circuits are often protected by keeper transistors, which regenerate logic states of noise-affected evaluation nodes by weak feedback. Here the analysis of noise tolerance metrics for dynamic circuits has been performed without the keeper transistor for two reasons. The design of the latch transistors in the keeper technique is ratioed, and the feedback transistors are sized so that it will supply enough current to cancel the effects of noise with a sacrifice of performance, such as, reduced speed, increased area, and increased power consumption. This transistor is not very fast, since the size of this transistor is kept as small as possible to limit the performance degradation. Consequently, discharge current due to large noise at the input of the PDN network can bring down the out voltage level before the weak feedback transistor can restore the logic level. Again, if the designers' goal is to make dynamic circuits robust against noise disturbance by utilizing keeper logic technique, the analysis of noise tolerance metrics of unguarded dynamic circuits will help to properly size the restoring feedback transistor.

4. Noise Scalability

Coupling is becoming stronger with technology scaling, and this stronger coupling is leading to higher noise injection, thereby degrading noise tolerance of CMOS digital integrated circuits. Most of the work in this area analyzed the noise effects from this conservative approach. This paper, however, emphasizes two important observations about noise scalability in dynamic circuits. While the overall scaling trends are making CMOS digital circuits

more susceptible to noise, there are two positive trends that actually help improve noise tolerance in dynamic circuits. Equation (2) shows that the induced noise voltage is linearly dependent on the supply voltage (V_{dd}), which is scaling down. Therefore, for a certain ratio of C_{CT}/C_{TOTAL} , the magnitude of the noise voltage will be decreased linearly with the supply voltage. In that sense, higher noise content due to increasing C_{CT}/C_{TOTAL} ratio can be counter balanced by decreasing supply voltage.

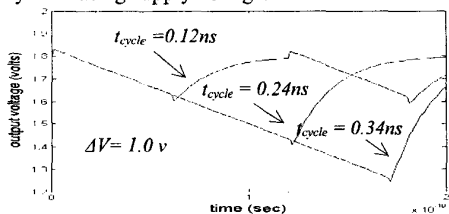


Fig. 10 Improving noise tolerance with increasing frequency

Second, since the frequency of CMOS technologies is continuously increasing, the available time to disrupt the logic level of any dynamic node is decreasing. So the output voltage change ($\frac{\Delta V}{C_L}$) due to a certain noise voltage ΔV will be less at higher

frequencies. Dynamic simulations (see Fig. 10) of the above example circuit with a constant $\Delta V = 1.0$ volts at three different frequencies show that the output voltage drop is lower at lower t_{cycle} . Therefore, noise tolerance of a dynamic circuit tends to improve with the increase of frequency, since a dynamic node can tolerate higher noise without functional failure as the cycle time goes down.

The static noise margin is a conservative measure of noise immunity for dynamic circuit, since the noise amplitude can safely be higher than threshold voltage at a lower clock cycle time, and noise content itself is lower at lower supply voltage. In addition the static approach ignores the fact that logic gates also acts as low-pass filters [4]. Therefore, adhering to the static noise margin could severely restrict the performance of a dynamic circuit. Since V_{dd} is scaling down by $1/s$ in current CMOS technologies, the noise content ΔV can be lowered if the C_{CT}/C_{TOTAL} ratio can be kept constant or scales up by a factor less than technology scaling factor s . Lowering the noise content is important, since load capacitance is being scaled down with technology scaling. At the same time the scaling down of V_m by $1/s$ decreases noise margins by $1/s$. Consequently, noises with shorter duration and smaller amplitude can cause logic failure. The negative effects of reduced load capacitance and smaller noise margins can be counter balanced to some extent by the increase of frequency by s , since higher frequency means less time to charge or discharge the capacitance responsible for holding logic level. Based on the above observations and assumptions, it can be inferred that noise in dynamic circuit can be made scalable to some degree. Here the analysis is presented based on the growing coupling between interconnect lines. However, it is important to consider various other factors, e.g., faster aggressor transition times, increased leakage current, process variations. Our future work will attempt to address these issues together with increasing coupling for comprehensive study of the scalability of noise in dynamic circuits.

5. Conclusion

Considering the increasing popularity of dynamic circuits, and the growing level of coupling between wires, this paper explored the issues of coupling noise in dynamic circuits. The proposed analytical solutions for noise as well as noise tolerance metrics closely estimate the behavior of a dynamic circuit under the

influence of coupling noise. The analytical expressions give results with around 5% margin of error. A more realistic approach is presented as compared to the conservative approach towards noise immunity. It is shown that to some degree noise can be made scalable with technology due to the linear dependency of noise level on the supply voltage and the C_{CT}/C_{TOTAL} ratio. It is also illustrated that increasing frequency improves noise tolerance by allowing dynamic circuits to tolerate higher noise levels.

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