

Possible Noise Failure Modes in Static and Dynamic Circuits

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Abstract: This paper investigates possible failure modes in both dynamic and static CMOS digital circuits due to noise disturbance. In current VLSI circuits, where mixture of static and dynamic implementation is very common, it is important to identify possible noise failure modes to help designers develop techniques to prevent such failures. Injection of noise causes temporary or permanent signal deviation on a circuit node depending on the level of noise and the affected circuit. The deviation of signal level of the circuit node may lead to functional failure in digital circuits, particularly in dynamic circuit families. Static circuits are inherently robust and can effectively restore the signal deviation before having undesired logic shift. However, some static circuits with a feedback loop cannot recover from noise-induced errors.

1. Introduction

With continuous scaling of feature sizes in deep submicron digital VLSI technologies, noise effects are having significant impact on circuit performance and signal integrity [1]-[4],[5]-[7]. A general CMOS circuit has input signals, output signals, internal static and dynamic nodes, and power and ground nodes on which noise can be injected from the various sources. Noise sources, that are most relevant to CMOS digital circuits, are (i) charge leakage and substrate noise, (ii) charge sharing noise, (iii) power and ground supply noise, and (iv) coupling or crosstalk noise [1]-[3]. With scaling of technology into the nano-meter regime the crosstalk due to capacitive and inductive coupling between neighboring lines is increasing, making circuits more liable to noise disturbance [5],[8],[9].

Whatever the sources or types of noise, the injection of noise into a circuit node causes a signal deviation at that node. This signal deviation will affect the operation of the circuit or circuit block driven by the victim net, and may lead to different kinds of unexpected behavior including functional failure or logic error. A functional failure is possible when an induced noise is propagated and wrongly evaluated at the primary output. The parameters that determine if there will be a logic error are (i) the amplitude and the duration of the noise pulse, (ii) the type of the victim node and the circuit connected to the victim node, and (iii) the signal condition on the affected node. In static circuits, momentary deviation of logic levels can be restored automatically, since at steady state the nodes are always connected either to ground or V_{dd} . But this restoration is not possible in dynamic circuits due to the possibility of having floating nodes [3],[5],[8],[9]. As a result the duration of the signal deviation may be equal to the length of clock pulse for dynamic circuits. However, in case of static circuits the signal deviation is always in the form of a glitch or a pulse with a small duration Δt (as illustrated in Fig.1). Consequently, dynamic circuits are more likely to suffer logic error due to noise disturbance. The worst-case scenario is when a dynamic victim node drives a dynamic gate. As opposed to dynamic circuits, static circuits are less likely to suffer from logic failure. However, static latches like *D flip-flops* have a feedback loop that cannot recover from noise-induced errors.

Since the impact of noise is becoming critical with scaling trends, it is important to detect possible modes of logic or functional

failure in different circuit families. The rest of the paper is organized as follows. Section 2 of this paper examines the modes of logic failure in combinational circuit families. Section 3 explores the possibility of logic failure in sequential circuits. Section 4 introduces an observation about increasing frequency and its effects on the probability of logic failure due to noise. Finally section 5 concludes the paper.

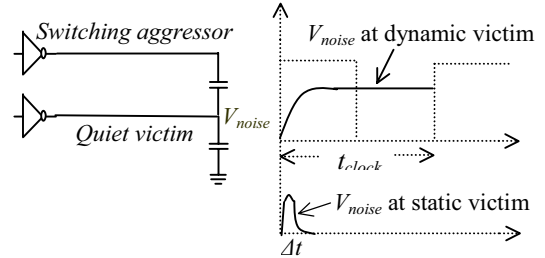


Fig.1. Effect of Noise on Static and Dynamic Nodes

2. Failures in Combinational Circuits

2a. Noise failures in dynamic combinational circuits

Dynamic gates are more liable to logic failure due to noise, since its DC noise margin is as low as the threshold voltage of the pull-down transistors. The failure due to noise at the input of a dynamic gate occurs when the signal deviation of the input victim net exceeds the DC noise margins of the following gate.

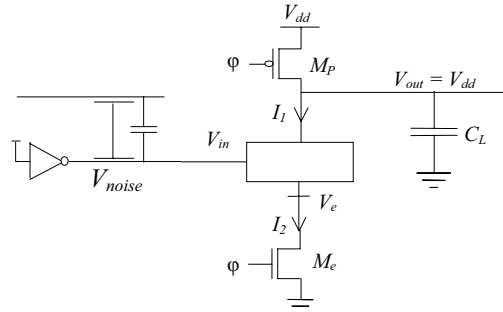


Fig.2 A dynamic inverter driven by a noise-affected line

If the victim net in Fig.1 drives a dynamic circuit (e.g. a dynamic inverter as in Fig.2) the injected noise (V_{noise}) will propagate through the dynamic circuit and affect its operation depending on the magnitude and the direction of V_{noise} . Two cases are considered: (i) victim node N is dynamic, and (ii) victim node N is static. In case of a dynamic victim node the duration of noise voltage V_{noise} is equal to the clock period. If the dynamic inverter in Fig.2 is pre-charged to V_{dd} and the magnitude of V_{noise} is slightly greater than the threshold voltage V_{tn} of the transistor M_n , the transistor M_n turns ON, and V_{out} starts to discharge. Analytical solution as in (1) [9] and simulation (see Fig.3 [9]) reveal that the discharge current I (where $I = I_1 = I_2$) depends almost linearly on the level of induced noise voltage V_{noise} .

$$I = p_c (V_{noise} - V_e - V_{tn})^\alpha \quad (1)$$

$$\text{where } V_e = p_v \left[\frac{V_{noise} - V_{e1} - V_{tm}}{(V_{dd} - V_{tm})^{1/2}} \right]^\alpha \text{ and } V_{e1} = \frac{V_{noise} - V_{tm}}{1 + \frac{1}{P_v}(V_{dd} - V_{tm})^{1/2}}$$

Here α is the velocity saturation constant; p_c is the constant that characterize the current drive capability of the transistor in the saturation region.

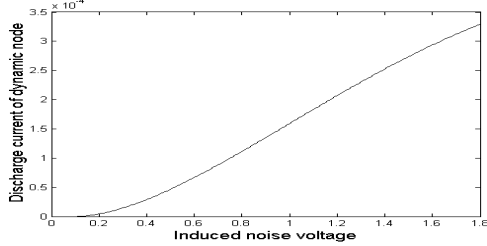


Fig.3 Discharge current I as a function of V_{noise} in a dynamic inverter driven by a dynamic victim net

The time required to discharge V_{out} is given by

$$t = \frac{V_{dd} - V_{out}(t)}{I} \cdot C_L \quad (2)$$

If the clock cycle is long enough to allow the discharge current I to bring down V_{out} below logic threshold, eventually there will be a functional failure (see Fig.4). Since the discharge current I depend almost linearly on V_{noise} , the circuit will have functional failure faster at higher level of V_{noise} . However, if the clock frequency of the driven dynamic circuit is very high so that the discharge current cannot sustain long enough to bring down V_{out} beyond the logic threshold, then higher level of V_{noise} can be tolerated without functional failure. Therefore, while a higher level of V_{noise} leads to faster functional failure of the driven dynamic circuit, higher frequency enables to tolerate higher V_{noise} by a dynamic circuit.

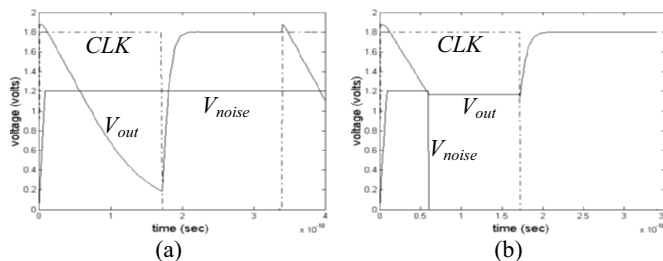


Fig.4 Signal deviation of a dynamic circuit driven by dynamic victim net

Now if the input victim net in Fig.2 is static, the discharge current stops as soon as the injected noise pulse disappears. Since the duration of a noise pulse on a static victim net is a small fraction of the clock cycle, the effect will not be as severe as that of a dynamic input victim net. Fig.4b shows that with a noise pulse of duration 0.5ns, having same amplitude as before, the change of V_{out} is much less than in the case of Fig.4a. It is important to note that in both cases the deviation of the signal level of the driven dynamic circuit cannot be restored to the original level although the effect in case of a static victim net is much less than the case of a dynamic victim net. Therefore the dynamic-dynamic combination is likely to have higher possibility of logic error than the static-dynamic combination. Noise pulses with higher amplitude and width on a static victim net may lead to a logic failure in the driven dynamic circuit.

2b. Noise failures in static combinational circuits

Due to the inherent robustness of static combinational circuits, the possibility of having functional or logic error by noise disturbance is very low. Since every static circuit node is always connected to either ground or V_{dd} , any signal deviation caused by the injected noise is restored quickly. To have a logic shift in such a node both the amplitude and the duration of the induced noise voltage have to be very large, which is very rare. If the same victim net as in Fig.2 drives a static inverter (see Fig.5), the deviation of V_{out} will be insignificant for the same noise contents compared to the cases of the dynamic inverter. If the driving victim net is dynamic in nature, for the same noise content as in Fig.4, the deviation of V_{out} is very small, and V_{out} settles at a level slightly lower than V_{dd} for the whole clock cycle (see Fig.6a). If the noise content is higher than the switching threshold of the driven static circuit, there may be a chance of logic failure. However, noise content in that case has to be much greater than the noise content in Fig.4 for the dynamic circuit. If the driving victim net is static in nature the change of V_{out} will be very small and temporary for the same noise content (see Fig.6b). This transient deviation vanishes quickly and V_{out} is restored to V_{dd} .

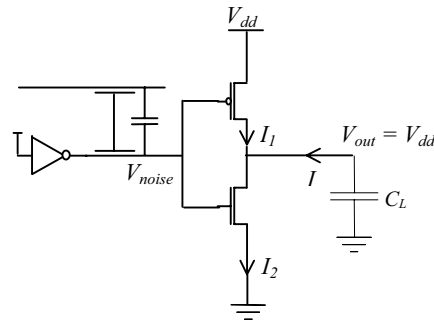


Fig.5: A static combinational circuit driven by a noise-affected line.

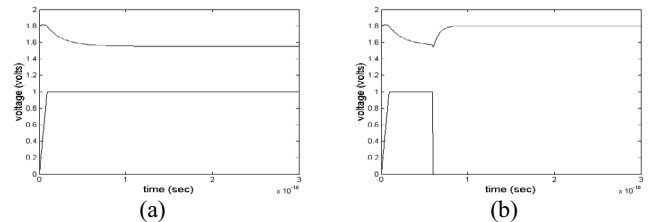


Fig.6 Signal deviation of a combinational static circuit driven by a dynamic victim net

The above analysis supports the fact that for static combinational circuits, the probability of having logic failure due to noise disturbance is extremely low as compared to dynamic combinational circuits.

3. Logic Failure in Sequential Circuits

3a. Noise failures in static sequential circuits

The main advantage of static logic over dynamic logic is its robustness under the influence of noise. But static logic may also suffer from logic failure if there is a feedback loop. Static D flip-flops (as in Fig.7), which are very common in registers, have a feedback loop that cannot recover from noise-induced errors. In these types of circuits there are three possible points where noise can be injected, which are the input, the clock, and the feedback loop. Among these three points the feedback loop is the most sensitive to noise. Even a small noise pulse on the feedback loop when the clock is falling or inactive will be propagated repeatedly through the loop and may ultimately destroy the logic information stored in the flip-

flop (see Fig.8). Fig.8 shows an unexpected shift of the logic levels of the D flip-flop in Fig.7 for a noise pulse of amplitude 0.9 volts and duration 0.2 ns.

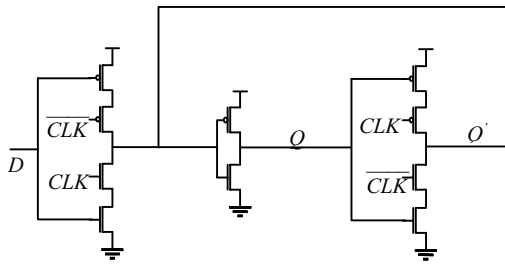


Fig.7 A simple D Flip-Flop: a common building block of register and storage unit.

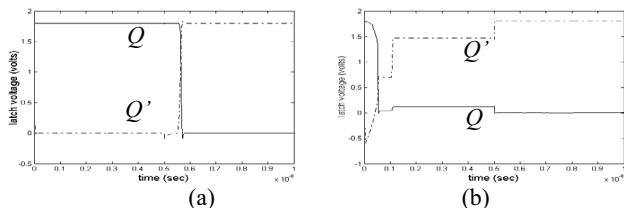


Fig.8: Functional failure in static D-latch. (a) Latch voltages at normal condition, (b) Logic error due to a small noise pulse of amplitude 0.9v and width 0.2ns.

3b Noise failures in dynamic sequential circuits

In case of static latches, the clock and the input are not that sensitive to noise as compared to the feedback loop. However, for dynamic latches both the clock and the input may become vulnerable to noise at different signal and switching conditions of the latches. For the two examples of dynamic latches in Fig.9, there is a very high probability of logic failure due to noise at the clock and the input lines.

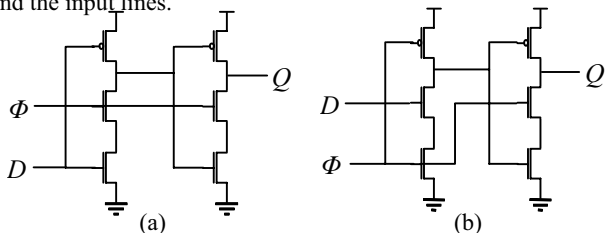


Fig.9 Two different versions of dynamic N latch []

If the input D of the latch in Fig.9a switches from high to low after the fall of the clock Φ the output Q will be dynamic high at normal operating condition (see Fig.10a). At this stage a small positive noise pulse on the clock line due to coupling with the aggressor net will change the logic state, and Q will be switched to "0" (see Fig.10b).

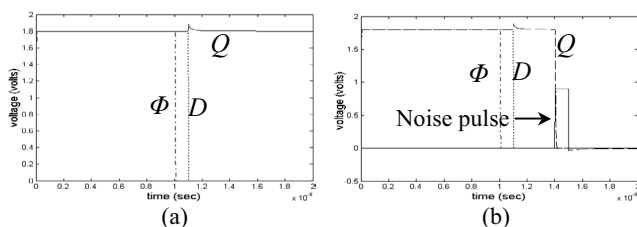


Fig.10: Noise sensitivity of dynamic latches. (a) Normal operating condition, (b) With a small noise pulse of amplitude 0.9v and width 1ns

Similarly if the input D of the same latch in Fig.9a switches from low to high after the fall of the clock (Φ) the output Q will be dynamic low. At this stage a small positive noise pulse on the clock line will change the logic state, and Q will be switched to "1". For the latch in Fig.9b the output Q is V_{dd} when $D = "1"$ and $\Phi = "1"$. If the input D falls after the fall of the clock Φ the output Q should still be dynamic high as illustrated in Fig.10a. A small positive noise pulse on the clock signal line from aggressor net will cause logic failure as in Fig.10b. Again if the D falls while the clock is high the output still should be dynamic high. A positive noise pulse on the low input may bring down the pre-charged output node Q . Although the input D of the latch in Fig.9b is sensitive to noise, its sensitivity is less than the clock.

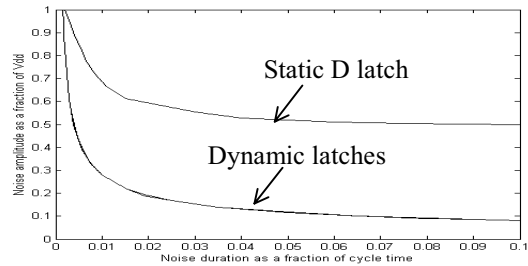


Fig.11 Comparison of noise immunity among three types of latch

Three noise immunity curves are presented in Fig.11 for the static D latch in Fig.7 and the two dynamic latches of Fig.9. Fig.11 plots the relative noise duration (D_r) against the relative noise amplitude (A_r). For the static D flip-flop noise pulses of various amplitudes and durations have been injected into the feedback loop, while keeping V_{dd} constant. For the dynamic latches the noise immunity curves are for noise on the clock. SPICE simulations were used to determine the set of noise amplitudes and durations that cause an undesired logic shift. The area above each curve in Fig.11 represents the amplitudes and durations of a noise pulse that can cause logic failure. The relative noise amplitude is defined as $A_r = A/V_{dd}$, where A is the amplitude of the noise pulse, and the relative duration of noise $D_r = D/C_f$, where D is the duration of the noise pulse and C_f is the cycle time. By comparing the noise immunity curves in Fig.11, it can be observed that dynamic latches are much more sensitive to noise than static latch.

4. Effect of increasing frequency on the possibility of logic error due to noise

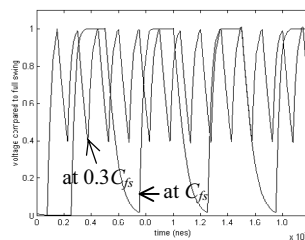


Fig.12 Voltage at a circuit node at two different frequencies

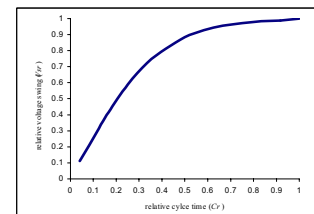


Fig.13 Decrease of voltage swing with the increase of frequency

It is important to note that with increasing clock frequencies, a circuit node may suffer from reduced voltage swing. That is, higher clock rate limits the achievable voltage swing at a circuit node (see Fig.12), since there is not enough time to fully charge or discharge the load capacitance. C_{fs} in Fig.12 is clock cycle time required to obtain the full voltage swing (V_{fs}) from zero to V_{dd} . Note that the supply voltage is not scaled here and is kept constant at V_{dd} . Fig.13

illustrates the decrease of voltage swing (V_s) with the decrease of clock cycle time (C). The clock cycle time and the voltage swing are normalized against the clock cycle at full swing (C_{fs}) and the full swing voltage (V_{fs}), respectively. The relative voltage swing is defined as $V_{sr} = V_s/V_{fs}$ and the relative cycle time $C_r = C/C_{fs}$. If the voltage swings changes all the signals become faster by the same ratio independent of the capacitive load at a circuit node. From the shape of this curve it is important to notice that the change of voltage swing slows down at longer clock cycle time. This shape correctly maps the change of actual signals on-chip with time. Any signal at a circuit node rises quickly at the beginning and as the signal reaches close to the full swing value it takes longer time for a certain change. Therefore, to reach higher voltage swings, the cycle time significantly increases. The curves in Fig.12 and Fig.13 have been produced by simulating a chain of gates driven by an inverter at different frequencies with constant supply voltage V_{dd} .

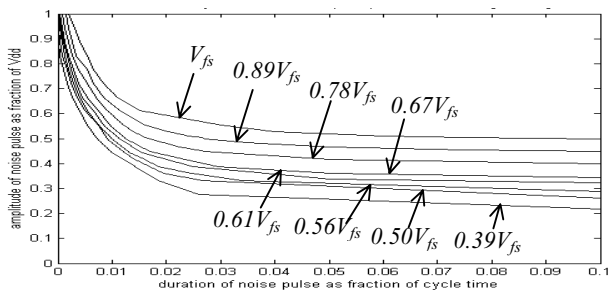


Fig.14 Noise immunity curves of a D flip-flop at various voltage swing

A circuit node is more likely to suffer from logic failure due to a certain level of noise with a reduced signal level. Therefore, increasing frequency leads to higher probability of logic failure at a circuit node due to reduced voltage swing. A set of noise immunity curves for the D flip-flop in Fig.7 is presented in Fig.14, which plots the relative noise duration (D_r) against the relative noise amplitude (A_r) at various voltage swings. Noise pulses of various amplitudes and durations have been injected into the feedback loop of a D flip-flop at different voltage swings, while keeping V_{dd} constant. The area above each curve in Fig.14 represents the amplitudes and durations of a noise pulse that can cause logic failure at a certain voltage swing. Hence, the lower the voltage swing the larger the area of noise amplitudes and durations that can cause an error. The highest curve is for the full voltage swing V_{fs} (swing from zero to V_{dd}). The lower curves illustrate noise immunity at voltage swings smaller than the full swing. The relative cycle time C_r is always less than 1 for lower voltage swings. Fig.15(a) plots the relative area above the noise immunity curve against the relative voltage swings (V_{rs}). It is observed that the area above the noise immunity curve increases with the decrease of the voltage swing, which means lower voltage swing leads to higher probability of logic error. The relation between cycle time and the area above the noise immunity curve in Fig.15(b) has been obtained by omitting the voltage swing variable from the two relations; cycle time versus voltage swing (Fig.13) and relative area above noise immunity curve versus voltage swing (Fig.15(a)). The curve in Fig.15(b), illustrates that higher frequency (smaller cycle time) leads to higher probability of logic error due to noise.

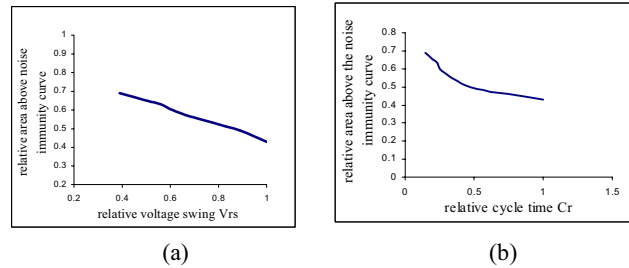


Fig.15 Relative area above noise immunity curve at various voltage Swings

5. Conclusion

This paper explores various scenarios, when signal deviation due to noise can cause logic failure in both dynamic and static circuits. Effects of noise on logic integrity are investigated for both combinational and sequential circuit families. As expected, it is shown that both combinational and sequential dynamic circuit families are much more vulnerable to noise disturbance compared to their static counterparts. Although static circuits are considered very robust against noise disturbance, it is shown that static circuit with a feedback loop may suffer from logic failure at certain situations. It has been observed that a circuit node may suffer from reduced voltage swing at higher frequencies, simply because, higher clock rate limits time to fully charge or discharge the load capacitance responsible for holding logic level at a circuit node. At a reduced voltage swing a circuit node is more liable to logic failure due to a certain level of noise. Therefore, this paper also illustrates the observation that increasing frequency may lead to higher probability of logic failure due to noise.

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