

Optimum Positioning Of Interleaved Repeaters In Bidirectional Buses

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ABSTRACT

It is shown in this paper that the optimum position of interleaved repeaters for minimum delay and noise is not the midpoint as commonly practiced. A closed form solution for the optimum position has been derived in this paper and verified by simulation. Bi-directional buses with the optimum interleaved repeater position are compared to commonly used bi-directional buses and shown to provide an improvement of as much as 100% in both the propagation delay and bit-rate per unit area. The area of the induced noise pulse on victim lines is shown to be zero indicating that the aggressor lines are virtually static when optimum repeater positioning is used.

Categories and Subject Descriptors

B.4.3 [INPUT/OUTPUT AND DATA COMMUNICATIONS]:
Interconnections (Subsystems) – *Topology(buses)*.

General Terms

Performance, Design.

Keywords

Buses, Delay, Noise, Interconnect, Repeaters.

1. INTRODUCTION

With the continuous scaling of technology, increased die area and faster clock speeds, the delay and noise of on-chip buses are becoming one of the main bottlenecks in current integrated circuits. The delay and noise through a long bus is a strong function of the coupling capacitance between the wires. Especially detrimental to delay is the Miller-like effect when adjacent wires simultaneously switch in opposite directions.

As the technology is scaled, the lateral component of interconnect capacitance (coupling capacitance) grows to dominate the total interconnect capacitance due to reduction in

wire pitch and the increase in the interconnects' aspect ratio. It is shown in [1] and [2] that in recent DSM technologies, the lateral interconnect capacitance components can be from three to five times as much as the vertical component. The growing coupling capacitance increases both the crosstalk between bus lines and hence deteriorates the signal integrity and the maximum bit-rate of the bus.

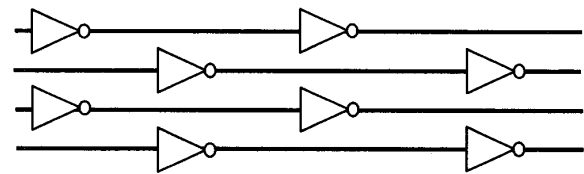


Fig. 1. Interleaved Repeaters on a Bus

In current bus design methodologies, designers interleave the position of the repeaters along each line to further reduce the delay due to coupling. A repeater on a unidirectional or a bi-directional bus line is usually positioned exactly midway between the positions of two consecutive repeaters on the adjacent bus line as shown in Fig. 1. This placement leads to a 50% reduction in the worst-case crosstalk delay compared to the delay of a bus without interleaved repeaters. This reduction is due to the fact that when half of the aggressor line switches in a certain direction, the other half switches in the opposite direction, significantly reducing the net coupling capacitance. Hence, the effective coupling capacitance between the aggressor and victim lines is reduced, leading to a reduction in both the propagation delay component due to crosstalk and the induced noise on the victim line.

The rest of the paper is organized as follows. In Section 2, the optimum interleaved repeater position is analytically derived. A comparison in propagation delay and noise is also performed between buses with optimal and midway repeater positions. In section 3, the performance of bi-directional buses with the optimal interleaved repeater positions, derived in section 2, is compared to other bi-directional buses commonly used in current integrated circuits. Finally, section 4 presents the conclusion.

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2. OPTIMUM INTERLEAVED REPEATER POSITION

In this section, the optimum interleaved repeater position is derived and shown to provide minimal propagation delay as well as zero area of the noise pulse induced on the victim net. The optimal positioning scheme will then be compared to the commonly used midway positioning scheme.

2.1. Optimum Interleaved Repeater Position for Minimal Propagation Delay

It is commonly and erroneously assumed that the optimum position of interleaved repeaters for minimum delay is the interconnect segment's midpoint. However, the optimum position for minimum delay, as is shown in this subsection, should be downstream of the segment's midpoint. This result can be explained by noting that the aim of interleaving the repeaters is to divide each segment into two parts coupled to segments switching in opposite directions. If the two parts have an equal share in the overall delay due to coupling, the total delay due to coupling can be cancelled. However, the coupling capacitance at the end of the line is driven by more resistance than that at the beginning of the line, and contributes more to the delay. Therefore, the point, at which the capacitance of each segment part equally contributes to the delay, will be downstream of the center of the segment.

Consider a two-line bus with interleaved repeaters as shown in Fig. 2. Repeaters are inserted along the lines to divide the lines into segments of length l . Repeaters on a line are positioned at a distance l' relative to the adjacent line repeaters. In order to get the Elmore delay at the end of segment 1 (between inverters a and b), we have to consider the coupling from segment 2 (right before inverter c on line 2) and segment 3 (right after inverter c on line 2). Thus, the Elmore delay, t_p , of segment 1 can be formulated as

$$t_p = 2.3 \times \left[\int_0^{l'} (R_{inv} + rx) \cdot (c_g + \alpha_{12} \cdot c_c) dx + \int_{l'}^l (R_{inv} + rx) \cdot (c_g + \alpha_{13} \cdot c_c) dx + (rl + R_{inv}) C_{inv} \right] \quad (1)$$

where r is the line's resistance per unit length, c_g is the line's vertical capacitance component per unit length and c_c is the line's lateral capacitance component per unit length. R_{inv} and C_{inv} are the repeater's output resistance and input capacitance, respectively. α_{12} is the switching activity coefficient between segments 1 and 2, while α_{13} is the switching activity coefficient between segments 1 and 3. α_{12} and α_{13} take the values shown in Table 1.

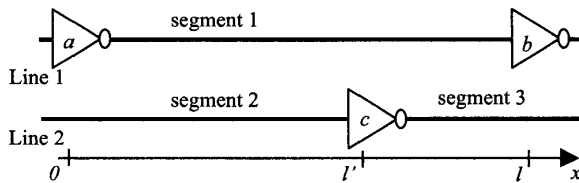


Fig. 2. Two adjacent bus lines with interleaved repeaters

Performing the integration in (1),

$$t_p = 2.3 \times \left[(rl + R_{inv}) C_{inv} + R_{inv} c_g l + \frac{rc_g l^2}{2} + \frac{rc_c}{2} \{ \alpha_{12} l^2 + \alpha_{13} (l^2 - l'^2) \} + R_{inv} c_c \{ \alpha_{12} l' + \alpha_{13} (l - l') \} \right] \quad (2)$$

Equation (2) can be rewritten as

$$t_p = t_{po} + t_{pc} \{ [\alpha_{12} \beta^2 + \alpha_{13} (1 - \beta^2)] + 2\eta_r [\alpha_{12} \beta + \alpha_{13} (1 - \beta)] \} \quad (3)$$

where

$$t_{po} = 2.3 \times \left[(rl + R_{inv}) C_{inv} + R_{inv} c_g l + \frac{rc_g l^2}{2} \right] \quad (4)$$

$$t_{pc} = 2.3 \times \frac{rc_c l^2}{2} \quad (5)$$

$$\eta_r = \frac{R_{inv}}{rl} \quad (6)$$

$$\beta = \frac{l'}{l}, \quad 0 < \beta \leq 1 \quad (7)$$

There are three possible switching scenarios for the two lines shown in Fig. 1, which results in the switching activity coefficients α_{12} and α_{13} listed in Table 1. Each of these cases has a different propagation delay equation as given in (8).

case 1:

$$t_{p11} = t_{po} + t_{pc} \{ 1 + 2\eta_r \}$$

case 2:

$$t_{p20} = t_{po} + t_{pc} \{ 2\beta^2 + 4\eta_r \beta \} \quad (8)$$

case 3:

$$t_{p02} = t_{po} + t_{pc} \{ 2(1 - \beta^2) + 4\eta_r (1 - \beta) \}$$

The worst-case propagation delay at any given interleaved repeater position will thus be

$$t_p(\beta) = \max(t_{p11}, t_{p20}, t_{p02}) \quad (9)$$

Table 1. Switching activity coefficients for different wire switching conditions

Switching Case	α_{12}	α_{13}
1. No activity on line 2	1	1
2. Segments 1 and 2 are switching in opposite directions	2	0
3. Segments 1 and 2 are switching in the same direction	0	2

Based on equation (9), the problem can be defined as: *It is required to find the optimum relative position ratio, β_{opt} , that minimizes the worst-case propagation delay in each of the switching possibilities of lines 1 and 2.*

Closely examining (8), there exists a certain value β_{opt} , such that when $\beta > \beta_{opt}$ then $t_{p20} > t_{p11}$ and $t_{p02} < t_{p11}$, while when $\beta < \beta_{opt}$ then $t_{p20} < t_{p11}$ and $t_{p02} > t_{p11}$. Thus,

$$\text{at } \beta = \beta_{opt}, \quad t_{p20} = t_{p02} = t_{p11} \quad (10)$$

Substituting from (8) into (10) gives

$$1 + 2\eta_r = 2\beta_{opt}^2 + 4\eta_r\beta_{opt} \quad (11)$$

Solving (11) yields

$$\beta_{opt} = 0.5 \times [\sqrt{(2\eta_r + 1)^2 + 1} - 2\eta_r] \quad (12)$$

$$\frac{1}{2} < \beta_{opt} < \frac{1}{\sqrt{2}} \quad (13)$$

Equation (12) shows that the optimal relative position ratio, β_{opt} , depends only on the resistive ratio η_r and varies from 0.5 to 0.707. When the inverter output resistance, R_{inv} , dominates the line resistance, rl , the resistance ratio η_r is very large and the propagation delay varies linearly with β , as shown in (3). This makes β_{opt} approach 0.5. At the other extreme, when the line resistance dominates the inverter output resistance, the resistive ratio η_r approaches zero and the propagation delay varies quadratically with β . This makes β_{opt} approach 0.707. In current DSM technologies the line resistance is usually comparable or higher than the repeater's output resistance. Thus, the optimum relative position ratio, β_{opt} will be closer to 0.707 rather than 0.5 as commonly assumed. The variation of β_{opt} with η_r , expressed by (12) is illustrated in Fig. 3.

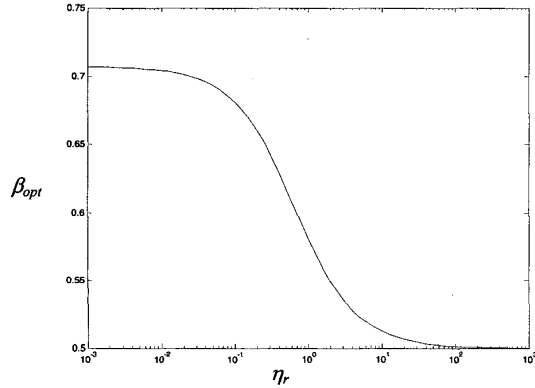


Fig. 3. Variation of β_{opt} with the resistance ratio η_r .

Substituting from (12) in (9), the optimum (minimal) propagation delay will thus be

$$t_{p,opt} = t_{po} + t_{pc} \{1 + 2\eta_r\} \quad (14)$$

The optimal propagation delay $t_{p,opt}$ given by (14) is exactly the same as the propagation delay, t_{p11} in (8), when line 2 has no activity. Thus, placing the interleaved repeaters at the optimal position $\beta_{opt}l$ causes adjacent lines to appear as virtual static lines independent of their switching condition.

2.2. Area of the noise pulse on the victim line:

In order to quantify the noise pulse on bus lines, consider the two adjacent bus lines in Fig. 2. Assume that line 1, the victim line, is quiet (has no switching activity), while the aggressor line, line 2, is switching. Then the area of the noise pulse induced on the victim line, [4], is

$$A = \int_{-\infty}^{\infty} v_1(t).dt = V_m \sum_k C_{cTk} R_k \quad (15)$$

where $v_1(t)$ is the instantaneous voltage induced on the victim line and V_m is the steady-state voltage of the segment on the aggressor line with the rising activity. C_{cTk} is the total coupling capacitance downstream of node k on the victim line and, R_k is the resistance of section k on the victim line.

Applying the integral form of the summation in (15) to the victim line in Fig. 2, we obtain

$$A = V_m \int_0^l (R_{inv} + rx).(\alpha_{12}.c_c) dx + V_m \int_l^l (R_{inv} + rx).(\alpha_{13}.c_c) dx \quad (16)$$

This integration evaluates to

$$A = V_m \left\{ \frac{rc_c}{2} [\alpha_{21}l^2 + \alpha_{31}(l^2 - l^2)] + R_{inv}c_c [\alpha_{21}l + \alpha_{31}(l - l)] \right\} \quad (17)$$

$$A = V_m t_{pc} \{ [\alpha_{21}\beta^2 + \alpha_{31}(1 - \beta^2)] + 2\eta_r [\alpha_{21}\beta + \alpha_{31}(1 - \beta)] \} \quad (18)$$

where t_{pc} , β and η_r are as defined in (5), (6) and (7), respectively.

Table 2. Switching Activity Coefficients for different switching conditions of segment 2

Switching Case	α_{21}	α_{31}
1. When segment 2 has a rising activity	1	-1
2. When segment 2 has a falling activity	-1	1

Each of the cases shown in Table 2, will have an area of its noise pulse given by

case 1:

$$A_1 = V_m t_{pc} \{ (2\beta^2 - 1) + 2\eta_r(2\beta - 1) \} \quad (19)$$

case 2:

$$A_2 = -A_1$$

In order to get a noise pulse with zero average voltage, we require a certain optimal relative position ratio, β'_{opt} , that will make $A_1 = -A_2 = 0$. Hence, equating (19) to zero yields

$$1 + 2\eta_r = 2\beta'^2_{opt} + 4\eta_r\beta'_{opt} \quad (20)$$

This result is exactly the same as (11) and hence the optimal relative position ratio, β'_{opt} , that gives a zero total area of the noise pulse of the victim line, is the same as the optimal relative position ratio, β_{opt} , that minimizes the propagation delay.

$$\beta'_{opt} = \beta_{opt} = 0.5 \times [\sqrt{(2\eta_r + 1)^2 + 1} - 2\eta_r] \quad (21)$$

Therefore, by positioning the interleaved repeaters at a relative position of $\beta_{opt}l$, both the propagation delay and the crosstalk induced on the line will be minimized. Since the area of the noise pulse is zero at optimal interleaved repeater positioning, the aggressor line acts as a virtual ground line.

2.3. Comparison to Midway Interleaved Repeater Positioning:

Positioning repeaters on a line exactly midway between any two repeaters on the adjacent line, i.e. $\beta=0.5$, will lead to a non-optimum propagation delay which can be obtained by substituting $\beta = 0.5$ in (9).

$$t_{p,mid} = t_{po} + t_{pc} \{1.5 + 2\eta_r\} \quad (22)$$

This delay is higher than the optimal delay by

$$\frac{\Delta t_p}{t_{p,opt}} = \frac{0.5 \times t_{pc}}{t_{po} + t_{pc} \{1 + 2\eta_r\}} \times 100 \quad (23)$$

The area of the curve in the case of $\beta = 0.5$ will also be non-optimal:

$$|A|_{mid} = 0.5 \times V_m t_{pc} > A_{opt} = 0 \quad (24)$$

Several simulations were performed on ELDO (a Mentor Graphics circuit simulation tool) to support the theory introduced in this paper. The simulation results in all the cases showed that the optimum worst-case propagation delay and the optimum area of the induced noise pulse occurred at a positioning exactly equal to the analytically derived β_{opt} . For example, a three-line bus was implemented in the Metal4 layer of a 0.18 μm TSMC CMOS technology. The repeaters were simple balanced inverters with an output resistance such that $\eta_r = 0.4$. By substituting in (12), $\beta_{opt} = 0.68$. The lines were simulated while varying the interleaved repeater position, β . The worst-case propagation delay on the middle line was recorded and plotted in Fig. 4. The simulation results show a minimum worst case delay at the calculated β_{opt} . The results also show that at the commonly used $\beta = 0.5$, the delay is 36% higher than the minimum delay at β_{opt} . Note that this percentage improvement in delay is not general but varies with the repeater and line characteristics as shown by (23).

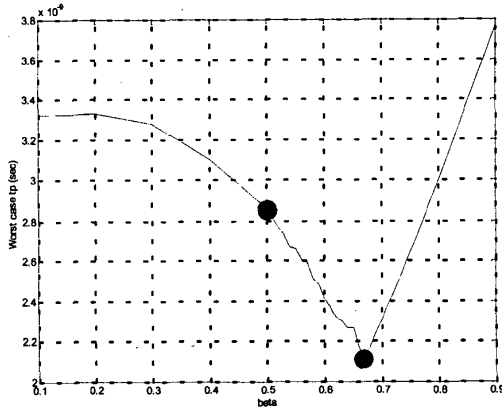


Fig. 4. Simulation results for worst-case propagation delay of the lines in Fig. 2, implemented in a METAL4 layer of a 0.18 μm CMOS technology.

The area of the noise pulse induced on the middle line, with the middle line inactive, was also recorded and plotted in Fig. 5. The area of the noise pulse diminished to zero at β_{opt} . It should

also be noted that the average area of the noise pulse at the commonly used $\beta = 0.5$, was significantly larger than zero as suggested by (24).

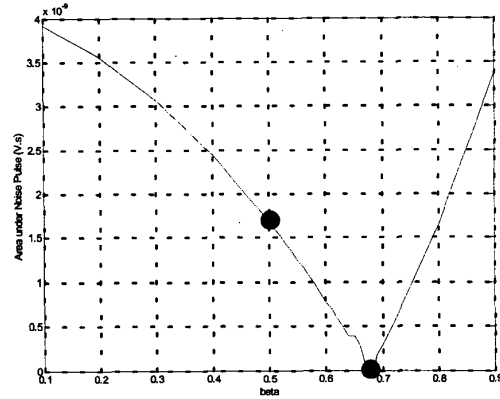


Fig. 5. Simulation results showing the area of the noise pulse for the lines in Fig. 2 implemented in a METAL4 layer of a 0.18 μm CMOS technology.

2.4. Practicality of the Optimal Interleaved Repeater Positioning Scheme

In the previous subsection, it was shown that inserting the interleaved repeaters at a relative position given by $\beta_{opt}l$ gives the optimum performance. This repeater positioning, however, cannot be practically applied to unidirectional buses. The reason can be explained based on the unidirectional two-line bus illustrated in Fig. 2. Even though placing inverter c at a relative distance $\beta_{opt}l$ from inverter a optimizes the performance on line 1, the relative position of inverter b with respect to inverter c is $(1 - \beta_{opt}) \times l \neq \beta_{opt}l$. Hence, although the performance of line 1 is optimized, the performance of line 2 will be degraded compared to midway positioning. Thus, the only solution to balance the performance of both lines is to place the interleaved repeaters midway between each two repeaters on the adjacent line, i.e. $\beta = 0.5$, as shown in Fig. 1. This is currently implemented in unidirectional buses.

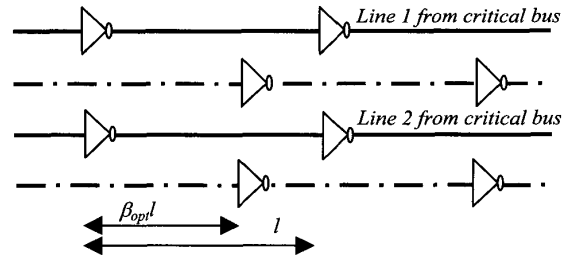


Fig. 6. Two buses combined together such that their lines alternate. Interleaved repeaters are inserted in both but optimally positioned on the lines of the critical bus to improve their performance

It is also worth mentioning that optimally positioned interleaved repeaters in unidirectional buses can improve the system performance if two neighboring buses exist, such that the delay of only one of them is critical. In that case, the two buses can be combined such that their lines alternate and the optimally positioned interleaved repeaters are placed such that the performance of the lines of the critical bus is improved. This case is illustrated in Fig. 6.

Although the optimal positioning of interleaved repeaters is not generally practical for unidirectional buses, but it can be efficiently implemented in bi-directional buses to improve their delay and noise performance. This is discussed in the following section and compared to other commonly used bi-directional buses. The previous analysis can be extended to derive the optimal positioning of interleaved repeaters in bi-directional buses. The main difference is that for each line the capacitive coupling to its *two* neighboring lines must be considered, which leads to a larger number of switching cases but yields the same previously derived optimum position (12).

3. BI-DIRECTIONAL BUSES WITH OPTIMALLY INTERLEAVED REPEATERS

In current integrated circuits, there are two main implementations of on-chip bi-directional buses. The first, shown in Fig. 7, is a set of lines with bi-directional buffers and static lines (ground or power lines) in between. The other bus implementation, shown in Fig. 8, is a set of lines with interleaved bi-directional repeaters inserted midway between any two repeaters on the adjacent line, $\beta=0.5$. In each of these two implementations, the data may flow in both directions on each of the signal lines but not simultaneously.

The bi-directional bus with optimally positioned interleaved repeaters is a set of unidirectional lines such that lines with opposite data flow alternate. Each line has interleaved repeaters inserted at the optimal relative position $\beta_{opt}l$, as illustrated in Fig. 9.

In order to fairly compare between the commonly used bi-directional bus implementations and the bi-directional bus with optimally positioned interleaved repeaters, a figure of merit M , defined, as the bit rate per bus area will be used. Also, the length per section l , the wire pitch s , and the used inverters are kept the same, and hence η_r , c_c and t_{pc} will remain the same.

$$M = \frac{B}{n \cdot (w+s) \cdot L} \quad (25)$$

where B is the bit rate of the bus, n is the number of bus lines, w is the physical width of the line, s is the signal line pitch and L is the length of the bus.

The bit rate is proportional to the reciprocal of the propagation delay and thus can be formulated as

$$B = \frac{\gamma}{t_p} n_s \quad (26)$$

where γ is a proportionality constant and n_s is the number of signaling bus lines. (25) can thus be rewritten as

$$M = \frac{\gamma n_s}{t_p \cdot n \cdot (w+s) \cdot L} \quad (27)$$

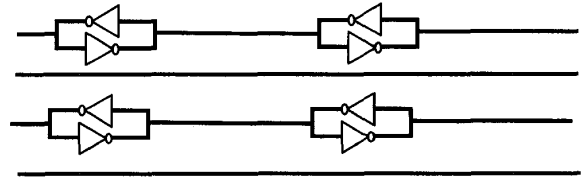


Fig. 7 Conventional bi-directional bus with static lines alternating with signal lines

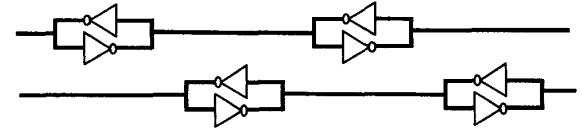


Fig. 8. Conventional bi-directional bus with midway positioned interleaved repeaters

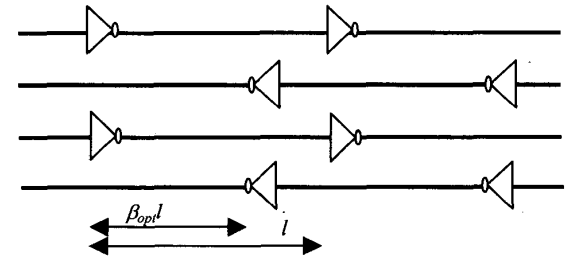


Fig. 9. Bi-directional bus with optimally positioned interleaved repeaters

The figure of merit for the bi-directional bus with optimally positioned interleaved repeaters, shown in Fig. 9, will be

$$M_0 = \frac{\gamma \cdot n}{t_{p,0} \cdot n \cdot (w+s) \cdot L} = \frac{\gamma}{t_{p,0} \cdot (w+s) \cdot L} \quad (28)$$

where $t_{p,0}$ is the optimum propagation delay of each line given by

$$t_{p,0} = t_{p,0,0} + 2t_{pc} \{1 + 2\eta_r\} \quad (29)$$

Note that this optimum propagation delay is the same as that defined in (14) but as each line is sandwiched between two lines, the coupling capacitance is doubled.

In the bi-directional bus implementation, shown in Fig. 7, the figure of merit will be

$$M_1 = \frac{\gamma \cdot n / 2}{t_{p,1} \cdot n \cdot (w+s) \cdot L} = \frac{\gamma}{2t_{p,1} \cdot (w+s) \cdot L} \quad (30)$$

where $t_{p,1}$ is the propagation delay of each line given by

$$t_{p,1} = t_{p,0,1} + 2t_{pc} \{1 + 2\eta_r\} \quad (31)$$

As the static line is not used for data signaling, only half of the bus lines are effectively sending data and hence $n_s = n/2$.

In the bi-directional bus implementation, shown in Fig. 8, the figure of merit will be

$$M_2 = \frac{\gamma \cdot n}{t_{p,2} \cdot n \cdot (w+s) \cdot L} = \frac{\gamma}{t_{p,2} \cdot (w+s) \cdot L} \quad (32)$$

where $t_{p,2}$ is the propagation delay of each line given by

$$t_{p,2} = t_{po,2} + 2t_{pc} \{1.5 + 2\eta_r\} \quad (33)$$

In addition, note that bi-directional repeaters [5] or boosters [6] implemented in the commonly used bi-directional buses have five to seven times the number of transistors in unidirectional repeaters. This implies that bi-directional repeaters and boosters have higher parasitics and thus, $t_{po,1} = t_{po,2} > t_{po,0}$. So by comparing (28) and (30),

$$\frac{M_0}{M_1} = \frac{2t_{p,1}}{t_{p,0}} = \frac{2[t_{po,1} + 2t_{pc} \{1 + 2\eta_r\}]}{t_{po,0} + 2t_{pc} \{1 + 2\eta_r\}} > 2 \quad (34)$$

M_0 is at least twice as M_1 . This indicates that the bi-directional bus with optimally positioned interleaved repeaters provides higher bit-rate per unit bus area. Moreover, the two buses have comparable noise performance since the adjacent lines to any signal line in the bi-directional bus with optimally positioned interleaved repeaters appear as virtual static lines and in the bus implementation shown in Fig. 7 each signal line is sandwiched between physically static lines.

By comparing (28) and (32),

$$\frac{M_0}{M_2} = \frac{t_{p,2}}{t_{p,0}} = \frac{[t_{po,2} + 2t_{pc} \{1.5 + 2\eta_r\}]}{t_{po,0} + 2t_{pc} \{1 + 2\eta_r\}} > 1 \quad (35)$$

M_0 will be higher than M_2 due to the optimum repeater positioning and the simpler unidirectional buffers used in the bi-directional bus with optimally positioned interleaved repeaters. Thus, the bi-directional bus with optimally positioned interleaved repeaters has a higher bit-rate per unit bus area than that of the bus implementation shown in Fig. 8. The amount of improvement will depend on the line and repeater parameters. Moreover, the noise performance of the bi-directional bus with optimally positioned interleaved repeaters is much better, since the area of the noise pulse induced on any line is zero as was discussed in the previous section.

4. CONCLUSION

Buses are one of the main bottlenecks in improving the performance of state-of-the-art integrated circuits. Several aspects of recent DSM technologies limit the maximum bit rate that can

be sent on the bus as well as degrading the signal integrity. In this paper, a new positioning scheme for the interleaved repeaters was introduced. The new positioning was shown to provide better propagation delay and noise performance than the commonly used midway positioning scheme.

Optimal interleaved repeater insertion was shown to be impractical in implementing unidirectional buses. However, bi-directional buses with optimally positioned interleaved repeaters showed superior performance in bit rate per unit area. The amount of improvement depends mainly on the characteristics of the bus lines and the repeater used and can exceed 100%, compared to common bi-directional buses. Moreover, with this optimum repeater placement, the area of the noise pulse of victim lines is zero indicating that aggressor bus lines are virtually static.

5. REFERENCES

- [1] P. P. Sotiriadis, A. Chandrakasan, "Bus Energy Minimization by Transition Pattern Coding (TPC) in Deep Sub-Micron Technologies," *ICCAD '00*, pp. 322-327, Nov. 2000.
- [2] Y. Shin, T. Sakurai, "Coupling-Driven Bus Design for Low-Power Application-Specific Systems," *38th DAC*, pp. 750-753, Jun. 2001.
- [3] S.P. Khatri, A. Mehrotra, R.K. Brayton, R.H.J.M. Otten, A. Sangiovanni-Vincentelli "A novel VLSI layout fabric for deep sub-micron applications," *36th DAC*, pp. 491-496, Jun. 1999.
- [4] Y. Ismail, "Evaluating Noise pulses in RC Networks due to Capacitive and Inductive Coupling," *ISCAS '02*, vol. 5, pp. 653-656, May 2002.
- [5] Hwang-Cherng Chow, "Bi-directional buffer for mixed voltage applications," *ISCAS '99*, pp. 270-273, vol. 1, May 1999.
- [6] A. Nalamalpu, S. Sirinivasan and W. Burleson, "Boosters for Driving Long On-chip Interconnects— Design Issues, Interconnect Synthesis, and Comparison with Repeaters," *IEEE Trans. on CAD*, vol. 21, No. 1, January 2002, pp. 50-62.