

Guest Editorial: Special Issue on On-Chip Inductance in High-Speed Integrated Circuits

THE appropriate interconnect model has changed several times over the past two decades due to aggressive technology scaling. New, more accurate interconnect models were introduced when parasitic effects that were negligible in earlier technologies, could no longer be ignored. Currently, RC models are used to analyze high resistance nets while capacitive models are used for less resistive interconnects. However, on-chip inductance is becoming increasingly important since integrated circuits now operate at frequencies where the inductive impedance of thick wide wires is comparable to wire resistance and line lengths are long enough, relative to signal rise times, for transmission line behavior to become significant.

Furthermore, this trend shows every indication of spreading beyond the relatively few lines it now affects. Operating frequencies that have increased dramatically over the past decade, are expected to maintain the same rate of increase over the next decade approaching 10 GHz by the year 2012. The use of thick upper level metals, large die sizes, and low resistance copper interconnect—already used in many commercial CMOS technologies, will likewise continue. Finally, because large die sizes enable more system integration, the use of long thick wide wires, once largely devoted to global clock distribution networks, will spread to critical data-buses and control lines.

This special issue deals with the design and analysis of integrated circuits including parasitic on-chip inductance. It does not deal with intentionally designed structures like the spiral inductors used in RF circuits and LC tank oscillators. As evidence that the subject material is still under investigation, the papers in this special issue do not present a unified approach to modeling parasitic inductance.

The most notable difference centers around the use of 2-D (or loop inductance) models versus more general 3-D inductance models, and at the center of this debate is the question of current loops formed by return currents. The 3-D model advocates take the position that the return current paths are fundamentally unknown and present sophisticated analysis methods to cope with the increased complexity of 3-D models. The 2-D advocates insist that the return currents are equal and opposite to the interconnect currents and can therefore, employ simpler models. While this debate is apparent in the second paper which favors 2-D models and the third, fourth, and sixth papers which favor 3-D models, several other papers also imply a preference by presenting analytical methods that are suitable to 2-D models only. The paper summary below highlights when notable, the authors stated or implied preference to 2-D or 3-D models.

In the first paper, Ismail presents several analytical methods for including inductive effects in both timing and noise analysis. The analytical models he presents are only applicable to

2-D loop inductance models. In the second paper, Kopcsay *et al.* review the basics of 2-D inductance modeling and introduce novel methods to include distant return paths and synthesize reduced-order circuit models that capture frequency dependent behavior.

The third, fourth, and fifth papers are exclusively devoted to 3-D models and methods to accelerate the use of 3-D models. In the third paper Beattie *et al.* describe the basic concepts on-chip magnetic interactions and review the more effective sparse approximations to 3-D inductance modeling such as equipotential shell methods and window based susceptance extraction. In the fourth paper, Gala *et al.* not only advocate sparse 3-D models for interconnect analysis they also investigate the influence of oftentimes ignored parasitics like device decoupling capacitances, device switching currents, and packaging effects. To handle the increased complexity they reformulate the PRIMA algorithm to produce a smaller, symmetric positive definite matrix suitable for Cholesky decomposition. The fifth paper by Hu *et al.* proposes two inductance extraction methods that consider other circuit characteristics to obtain highly sparsified and accurate inverse inductance matrices. The second algorithm folds away the power/ground network in a manner the editors find somewhat similar to 2-D loop inductance formulations. Their paper also describes K-PRIMA, their extension of the PRIMA algorithm that handles inverse inductance, or K, matrices.

The sixth paper by Mezhiba *et al.* investigates the inductive properties of different power grid designs. It explores the trade-offs of inductance/area/resistance in allocating metal resources. The seventh paper by Svensson reviews the performance of electrical interconnects including inductance and skin effect and finds delays, data rates, and power consumption are on par or superior to optical interconnects. The analytical methods Svensson employs are necessarily linked to 2-D models. In the eighth paper Massoud *et al.* explore design techniques such as shielding, widening lines, increased line separation, buffer insertion, differential signaling, and dedicated ground planes to reduce on-chip inductive effects. In the ninth and final paper, Cao *et al.* precharacterize interconnect/power grid/circuit interactions to derive an effective-inductance lookup table suitable for timing analysis and buffer insertion.

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Yeah I. Ismail (M'00) was born in Giza, Egypt, on November 11, 1971. He attended the School of Engineering, Department of Electronics and Communications at Cairo University, Egypt, from 1988 to 1993, where he received the B.Sc. degree in electronics and communications engineering with distinction and honors. As one of the top of his class, he was appointed as a teacher assistant at the Department of Electrical and Computer Engineering, Cairo University in August 1993. He received his first Masters degree in electronics from Cairo University (distinction), in June 1996. In September 1996, he attended University of Rochester, Rochester, NY, where he received his second Masters degree in electrical engineering from the in 1998 and the Ph.D. degree in April 2000.

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Prof. Ismail has won the 2002 IEEE Circuits and Systems Society Outstanding Young Author Award and has also won the National Science Foundation Career Award in 2002. He is on the editorial boards of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: FUNDAMENTAL THEORY AND APPLICATIONS.



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