Performance Analysis of Deep Sub micron VLSI Circuits in the Presence of Self and Mutual Inductance

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Abstract *- This paper illustrates the growing significance of self and mutual inductances by examining their effects on performance and characteristic issues like propagation delay, rise time, and overshoots. This paper introduces Elmore-like closed form solutions to analyze the behavior of integrated circuits in the presence of self and mutual inductances. The complexity of the expressions introduced here is linear with the number of elements in the interconnect network, and has an Elmore delay accuracy characteristics. The propagation delay and overshoots estimated based on these formulae are within 15% of AS/X simulations for a wide range of interconnects from IBM's most recent CMOS technology.*

I. Introduction

In current deep sub-micrometer CMOS technologies interconnect parasitic elements are dominating factors of integrated circuits performance [1]-[16]. Recent CMOS technologies using low resistance metals for interconnects such as copper [7], [8] and higher operating frequencies make it crucial to include the self and mutual inductances in the interconnect model. With the introduction of self and mutual inductances in modeling interconnect lines, performance analysis becomes significantly more complex as compared to standard *RC* modeling [3]-[6], [10]-[12]. This complexity is aggravated by the fact that a line can inductively couple to a large number of lines. To quickly estimate the circuit behavior such as propagation delay, oscillations, and overshoots in the presence of self and mutual inductances, a set of simple closed form expressions would be of great importance.

The rest of the paper is organized as follows. Section II of this paper illustrates the effects of the self and mutual inductances with three sets of AS/X [9] simulation results based on IBM's most recent CMOS technology. A set of closed form expressions, which can handle inductively and capacitively coupled trees are introduced in section III. These expressions have linear complexity with the number of elements in the interconnect network and an Elmore delay accuracy characteristics [6], [13]. This section also compares the results of simulations with the values estimated by the proposed formulae. Conclusions are provided in section IV and the derivation of the moments of inductively and capacitively coupled trees is presented in the appendix.

II. Effects of Self and Mutual Inductances

Three sets of AS/X [9] simulation results are presented based on IBM's most recent technologies to illustrate the importance of on-chip self and mutual inductances. The first example is a 4-bit coupled bus (see Table 1). The second example is a tree coupled with two lines (see Table 2). The third example is a pair of lines coupled with each other (see Table 3). In all three examples simulations are done for three cases. In case I, self and mutual inductances are not included. That is, signal lines are considered as standard *RC* lines with coupling capacitances only. In case II, self-inductance is included, and lines are considered as *RLC* lines with coupling capacitance, but no coupling inductance. In case III, both self and mutual inductances are included and lines are considered as *RLC* lines with coupling capacitance and mutual inductance. Results show that the error due to neglecting inductance can be more than 100% for the delay calculation and 70% in the rise time. Hence, it is imperative to include self and mutual inductances in the interconnect modeling for proper fault free VLSI circuit analysis [15]-[19].

Table 1: AS/X simulation of a 4-bit BUS.

BUS	All lines are switching in the same direction.				
	Case			% Deviation	
	I	II	III	I- III	II-III
Delay	29.32	44.2	58.67	100	33
Rise Time	84.59	25.5	26.81	68.3	5.14
% Overshoot	0	10.3	23.79	-	126
Time of overshoot	-	115	155.2	-	35.3

Table 2: AS/X simulation of a coupled tree network

TREE	All lines are switching in the same direction.				
	Case			% Deviation	
	I	II	III	I- III	II-III
Delay	30.46	43.59	51.98	71.5	18.5
Rise Time	87.1	43.36	37.29	58.6	13.4
% Overshoot	0	7.2	15	-	108
Time of overshoot	-	113.4	134	-	18.2

Table 3: AS/X simulation of a pair of coupled lines

LINE	All lines are switching in the same direction.				
	Case			% Deviation	
	I	II	III	I- III	II-III
Delay	63.12	74.13	83.64	32.53	12.83
Rise Time	147.8	85.36	49	67	43
% Overshoot	0	0.74	6.2	-	737
Time of overshoot	-	269	221.5	-	17.69

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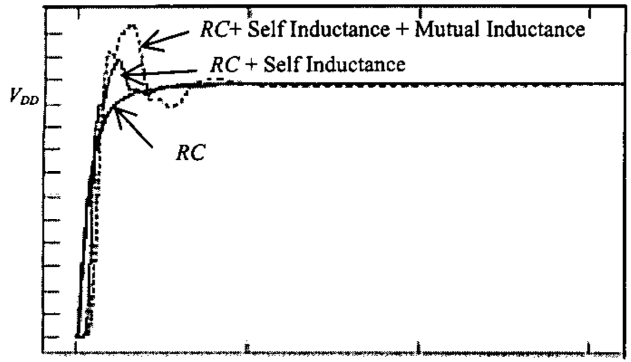

Fig. 1. Signal behavior on one net of a 4-bit BUS

III. Closed Form Expressions in the Presence of Self and Mutual Inductances

A second order system is derived as an approximation of the interconnect transfer function at any node. Signal characteristics such as delay and overshoots are characterized in closed form based on the second order approximation given by [6]

$$g(s)=\frac{\omega_n^2}{s^2+s2\zeta\omega_n+\omega_n^2}. \qquad (1)$$

The transfer function in (1) can be expanded in powers of s as,

$$g(s)=1-s\left(\frac{2\zeta}{\omega_n}\right)+s^2\left(\frac{-1+(2\zeta)^2}{\omega_n^2}\right)-\ldots, \qquad (2)$$
$$=1+m_1 s+m_2 s^2+\ldots..$$

where the first two moments of the transfer function are equated to the first two moments of the system, m_1 and m_2. Hence, the parameters that characterize the second order approximation (damping factor ζ and natural frequency ω_n) can be calculated in terms of the first two moments of the system as given by

$$\zeta=\frac{-m_1}{2}\frac{1}{\sqrt{m_1^2-m_2}} \quad \text{and} \quad \omega_n=\frac{1}{\sqrt{m_1^2-m_2}} \qquad (3)$$

To calculate ζ and ω_n, the first and second moments of the system need to be calculated. It is shown in the appendix that the first and the second moments of the transfer function at node i of a set of inductively and capacitively coupled trees are given by expressions (4) and (5), respectively. See the appendix for the detailed derivation of these formulae.

$$m_{1,i}=-\sum_k\left[R_k\cdot\sum_{r,j}C_{rj}\cdot(\alpha_r-\alpha_j)\right] \qquad (4)$$

$$m_{2,i}=-\sum_k\left[R_k\cdot\sum_{r,j}C_{rj}\cdot(m_{1,r}-m_{1,j})\right]-\sum_k\left[\begin{array}{l}L_k\cdot\sum_{r,j}C_{rj}\cdot(\alpha_r-\alpha_j)\\+M_k\cdot\sum_{l,m}C_{lm}\cdot(\alpha_l-\alpha_m)\end{array}\right], \qquad (5)$$

where k runs over all the branches on the path from the primary input to node i on the tree which i belongs to; r runs over all the nodes downstream of k on that tree, and j runs over all the nodes to which r has a capacitance connected to. In the case of capacitances to ground, $j = 0$. The index l runs over all the nodes downstream of M_k **on the coupled tree** (which i does not belong to). The index m runs over all the nodes which l has a capacitance connected to. See the appendix for an example of how to calculate these expressions.

Each line has a switching factor associated with it and is denoted α_i for interconnect i. The switching factor takes the values 1, 0, and −1 for lines switching from low-to-high, non-switching lines, and lines switching from high-to-low, respectively. Substituting the moments of (4) and (5) in (3), the expressions in (6) for the damping factor and natural frequency result, where τ_{RC} and τ_{LC} are given by (7) and (8), respectively. These formulae are simple, recursive, and can be calculated in linear time with the number of elements in the network.

$$\zeta=\frac{1}{2}\frac{\tau_{RC}}{\tau_{LC}} \quad \text{and} \quad \omega_n=\frac{1}{\tau_{LC}}, \qquad (6)$$

$$\tau_{RC}=\sum_k\left[R_k\cdot\sum_{r,j}C_{rj}\cdot(\alpha_r-\alpha_j)\right] \qquad (7)$$

$$\tau_{LC}=\sqrt{\sum_k\left[\begin{array}{l}L_k\cdot\sum_{r,j}C_{rj}\cdot(\alpha_r-\alpha_j)\\+M_k\cdot\sum_{l,m}C_{lm}\cdot(\alpha_l-\alpha_m)\end{array}\right]} \qquad (8)$$

Note that the approximation that $(m_{1,i})^2$ is equal to the first term of $m_{2,i}$ has been used. This same approximation is used in Elmore and Wyatt delay models [13], [14] and in the equivalent Elmore delay model [6], and is particularly accurate in the case of balanced interconnect structures as explained in [6]. Once the damping factor and natural frequency are determined at a certain node for an arbitrary switching pattern, the propagation delay, and the percentage overshoots can be determined for step inputs as described in [6]. The expressions for propagation delay and percentage overshoots are given by (9) and (10), respectively, where t_{pdi} is the propagation delay at node i and $\%O_i$ represents the maximum overshoots due to oscillation for n odd and minimum undershoots for n even at node i.

$$t_{pdi}=(1.047e^{-\frac{\zeta_i}{0.85}}+1.39\zeta_i)/\omega_{ni} \qquad (9)$$

$$\%O_i=(-1)^{n+1}\cdot 100\exp\left(-\frac{n\pi\zeta_i}{\sqrt{1-\zeta_i^2}}\right) \quad n=1,2,\ldots \qquad (10)$$

Table 4 compares the delay from AS/X simulations with the delay values calculated by the approximate expressions. In almost all the cases the delay formula estimates the propagation delay within less than 10% margin of error. Table 5 presents a comparison for the percentage maximum overshoot. The overshoot formula estimates percentage maximum overshoot closely for all the three examples, for the case when lines are modeled as distributed *RLC* with capacitive and inductive coupling. The error in this case is within 15%.

Table 4: Delay– simulation vs. approximation

Case		BUS	Tree	Line
I	Simulation	29.32	30.46	63.11
	Approximation	31.64	29.20	66.12
	Margin of error	7.9%	4.14%	5%
II	Simulation	44.14	43.59	74.13
	Approximation	41.06	45.02	81.50
	Margin of error	7%	3.28%	10%
III	Simulation	58.67	51.98	83.64
	Approximation	50.8	51.00	87.00
	Margin of error	13%	1.89%	4%

Table 5: %overshoot– simulation vs. approximation

Case		BUS	Tree	Line
III	Simulation	23.80	15	6.2
	Approximation	27.36	13.56	5.45
	Error	15%	10%	12%

IV. Conclusion

It is shown in this paper that in analyzing VLSI circuits if standard distributed *RC* models are used ignoring inductive effects, large errors occur in the prediction and evaluation of the circuit behavior. It is observed that the self and mutual inductances affect deep sub-micron VLSI circuit performance by increasing signal propagation delay and oscillations, and decreasing rise time at any given input switching condition. The closed form expressions presented here give results fairly close to simulation data (within 15% of AS/X) and can be evaluated in a time comparable to Elmore delay.

Appendix: Moments Calculation for Inductively and Capacitively Coupled *RLC* Trees

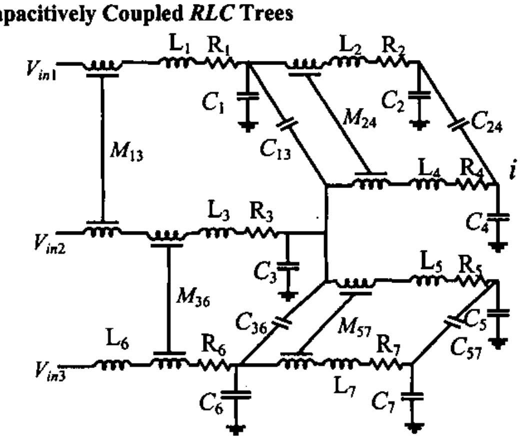

Fig. 2. An RLC interconnect network with capacitive and inductive coupling

For any interconnect structure, if after removing the inductive and capacitive coupling all that remains is a set of *RLC* trees and lines, this structure is considered a tree based structure. An example is the circuit in Fig. 2, where if inductive and capacitive coupling are removed, a tree and two lines remain. For such capacitively and inductively coupled *RLC* trees, the moments of the response at different nodes can be calculated in linear time using simple recursive formulae. Capacitively and inductively coupled trees have multiple inputs. The case is considered here when all the inputs have the same waveform shape but are not necessarily switching in the same direction. The waveform shape is arbitrary. For a node i where the moments are being calculated, the input with a DC path to i is called the primary input. For example, the primary input for node i in Fig. 2 is V_{in2}. V_{in1} and V_{in3} have no DC path to node i since both capacitive and inductive coupling are open circuit at DC.

Consider calculating the moments at node i of Fig. 2, a capacitively and inductively coupled tree structure. The voltage at node i can be expressed as

$$V_i(s)=V_{inp}(s)-\sum_k\left[(R_k+sL_k)\sum_{r,j}C_{rj}s(V_r(s)-V_j(s))\right] -\sum_k sM_k\sum_{l,m}C_{lm}s(V_l(s)-V_m(s)) \qquad (11)$$

where k runs over all the branches on the path from the primary input to node i on the tree which i belongs to; r runs over all the nodes downstream of k on that tree, and j runs over all the nodes to which r has a capacitance connected to. In the case of capacitances to ground, $j = 0$. V_{inp} is the primary input for node i. For example, in Fig. 2, there are two resistances, R_3 and R_4, from the primary input to node i. Hence, k runs over R_3 and R_4, L_3 and L_4, and the mutual inductances M_{13}, M_{36}, and M_{24}. The index l runs over all the nodes downstream of M_k **on the coupled tree** (which i does not belong to). The index m runs over all the nodes which l has a capacitance connected to.

The above formula can be understood by noting that the summations

$$\sum_{r,j}C_{rj}s(V_r(s)-V_j(s)) \text{ and } \sum_{l,m}C_{lm}s(V_l(s)-V_m(s)) \qquad (12)$$

represent the currents flowing out of nodes k and l, respectively. The term

$$(R_k+sL_k)\sum_{r,j}C_{rj}s(V_r(s)-V_j(s)) \qquad (13)$$

in Fig. 2 represents the voltage drop between the primary input and node i due to the current flowing out of node k. Note that the node k belongs to the same tree as i since it is this current that has to run through R_k and L_k. The term

$$sM_k\sum_{l,m}C_{lm}s(V_l(s)-V_m(s)) \qquad (14)$$

represents the voltage drop between the primary input and node i due to the current flowing out of node l causing a voltage drop between the primary input and node i due to the mutual inductance M_k. The voltage drop at node a due to inductive coupling between two branches a and b is given by M_{ab}x i_b' where i_b' is the rate of change of the current passing **through branch *b***. Hence, voltage drops can occur at node i due to the current at nodes that are not in the same tree as i due to inductive coupling as described by (14). By expanding the voltages in (11) into powers of s given by

$$\begin{aligned} V_i(s)&=\frac{m_{0,i}}{s}+m_{1,i}+m_{2,i}s+m_{3,i}s^2+\ldots \\ V_{inp}(s)&=\frac{m_{0,inp}}{s}+m_{1,inp}+m_{2,inp}s+m_{3,inp}s^2+\ldots \qquad (15) \\ V_k(s)&=\frac{m_{0,k}}{s}+m_{1,k}+m_{2,k}s+m_{3,k}s^2+\ldots \\ &\vdots \end{aligned}$$

and comparing similar powers of s on both sides of (11), the following relations result

$$m_{0,i} = m_{0,inp}$$

$$m_{1,i} = m_{1,inp} - \sum_k \left[R_k \sum_{r,j} C_{rj}(m_{0,r} - m_{0,j}) \right]$$

$$m_{n,i} = m_{n,inp} - \sum_k \left[R_{rk} \sum_{r,j} C_{rj}(m_{n-1,r} - m_{n-1,j}) \right] - \sum_k \left[L_k \sum_{r,j} C_{rj}(m_{n-2,r} - m_{n-2,j}) \right] - \sum_k \left[M_k \sum_{l,m} C_{lm}(m_{n-2,l} - m_{n-2,m}) \right] \text{for } n = 2,3, \tag{16}$$

These relations allow calculating all the moments recursively in linear time. Note that the moments of the inputs are known since the inputs are given. For example, if the input signal is given by

$$V_{inp} = 1 - e^{-\frac{t}{T}} \tag{17}$$

the moments are given by $m_{0,inp} = 1$, $m_{n,inp} = T^n$. For a step input, $m_{o,\,inp} = 1$, $m_{n,\,inp} = 0$.

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